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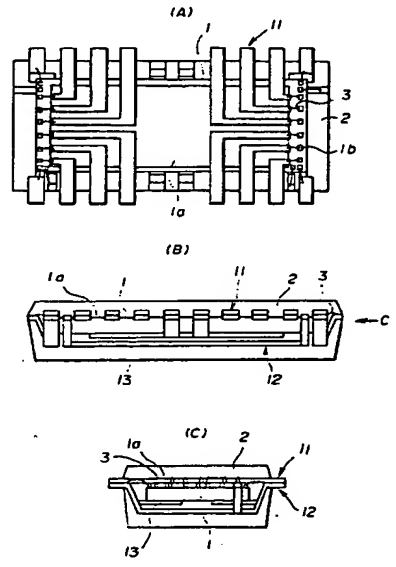
(54) Semiconducter device and method of producing the same

(57) A semiconductor device includes a semiconductor chip (1) having top and bottom surfaces, upper leads (11) electrically coupled to the semiconductor chip, where a first gap is formed between the upper leads and the top surface (1a) of the semiconductor chip, lower leads (12) electrically coupled to the semiconductor chip, where a second gap is formed between the lower leads and the bottom surface of the semiconductor chip, and an encapsulating resin (2) which encapsulates the semiconductor chip so as to maintain the first and second gaps.

FIG.4



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention generally relates to semiconductor devices and methods of producing the same, and more particularly to a semiconductor device which is resin encapsulated and to a method of producing such a resin encapsulated semiconductor device.

[0002] Recently, although the size of the semiconductor chip of the resin encapsulated semiconductor device has increased, there are demands to reduce the size of the package itself. However, in the existing semiconductor device which uses the lead frame having the two-dimensional structure, there is a limit to reducing the size of the package. Furthermore, when the size of the package is reduced to the limit, there are problems in that the mechanical strength, reliability and the like of the semiconductor device deteriorate.

[0003] Accordingly, there are proposals to use the top or bottom surface of the semiconductor chip which was conventionally unused by arranging the leads on the top or bottom surface of the semiconductor chip, so that the leads have a three-dimensional structure. The COL (Chip on Lead) and the LOC (Lead on Chip) are examples of such a three-dimensional structure, and a Japanese Laid-Open Patent Application No.61-218139 proposes such a three-dimensional structure.

[0004] FIG.1 shows an example of a conventional semiconductor device having the COL structure. In FIG.1, (A) shows a plan view of the semiconductor device with a part of an encapsulating resin omitted, and (B) shows a front view of the semiconductor device with a part of the encapsulating resin omitted.

[0005] In FIG.1, inner leads 4 are arranged in a predetermined shape, and a stepped part is provided at a part where a semiconductor chip 1 is mounted. The semiconductor chip 1 is fixed above the inner leads 4 via an insulator 6. Electrodes of the semiconductor chip 1 and ends of the inner leads 4 are connected via bonding wires 3, and the entire semiconductor device excluding outer leads 5 are packaged by an encapsulating resin 2.

[0006] Hence, according to the COL structure, the inner leads 4 run on the lower side of the semiconductor chip 1 to form the package having the three-dimensional structure.

[0007] FIG.2 shows an example of a conventional semiconductor device having the LOC structure. In FIG.2, (A) shows a plan view of the semiconductor device with a part of the encapsulating resin omitted, and (B) shows a front view of the semiconductor device with a part of the encapsulating resin omitted. In FIG.2, those parts which are essentially the same as those corresponding parts in FIG.1 are designated by the same reference numerals, and a description thereof will be omitted.

[0008] In FIG.2, the insulator 6 is provided on the semiconductor chip 1, and the inner leads 4 are arranged on top of the insulator 6. The ends of the inner leads 4 and the electrodes of the semiconductor chip 1 are connected via the bonding wires 3, and the entire semiconductor device excluding outer leads 5 are packaged by an encapsulating resin 2.

[0009] Hence, according to the LOC structure, the inner leads 4 run on the upper side of the semiconductor chip 1 to form the package having the three-dimensional structure.

[0010] However, according to the COL and LOC structures, the inner leads 4 run only on the lower or upper side of the semiconductor chip 1, and this arrangement is insufficient for efficiently providing the necessary wiring for a more complex circuit.

[0011] In addition, the insulator 6 must be provided between the semiconductor chip 1 and the inner leads 4. If the matching of this insulator 6 and the encapsulating resin 2 is poor or the adhesion between the insulator 6 and the encapsulating resin 2 is insufficient, there is a problem in that a crack is easily formed in the encapsulating resin 2 after the packaging. If such a crack is formed in the encapsulating resin 2, the reliability of the semiconductor device greatly deteriorates.

[0012] Furthermore, particularly in the case of the LOC structure, the insulator 6 provided on the circuit forming surface of the semiconductor chip 1 is a thin insulator film, and the inner leads 4 arranged on this thin insulator film is made of a metal having a large coefficient of linear expansion. For this reason, the inner leads 4 undergo a large expansion when the semiconductor device operates and the semiconductor chip 1 generates heat, and a large difference is introduced between the expansion of the semiconductor chip 1 and the expansion of the inner leads 4. A stress is generated at the surface of the semiconductor chip 1 due to this difference in the expansions, thereby applying forces on and deforming the circuits within the semiconductor chip 1.

[0013] An improved semiconductor device shown in FIG.3 having the LOC structure was thus proposed in a Japanese Laid-Open Patent Application No.59-66157 (Published Application No.4-1503). In FIG.3, (A) shows a cross-sectional side view of the semiconductor device, (B) shows a plan view of a lead frame, and (C) shows a plan view of a stage frame.

[0014] In FIG.3, a lead frame 8 includes inner leads 4 and outer leads 5 which are formed to predetermined shapes and connected to a frame 15. On the other hand, a stage frame 9 includes a rectangular stage 13 which is connected to a central position of the frame 15 via a bent part 10 which forms a step relative to the frame 15.

[0015] As shown in FIG.3, the semiconductor chip 1 is mounted on the stage 13, and the packaging is made by the encapsulating resin 2 after overlapping the lead frame 8 and the stage frame 9. In this state, the semiconductor chip 1 and the inner leads 4 are mutually separated by the provision of the bent part 10 in the stage

frame 9. Accordingly, the semiconductor chip 1 and the inner leads 4 are isolated by the encapsulating resin 2 which exists therebetween. As a result, the problems caused by the provision of the insulator 6 in the semiconductor device shown in FIG.2 are eliminated because the semiconductor device shown in FIG.3 does not require the insulator 6.

[0016] However, because the bent part 10 for forming the gap between the semiconductor chip 1 which is mounted on the stage 13 and the inner leads 4 is provided inside the package, there is a new problem in that the size of the package cannot be made less than or equal to a sum of the size of the semiconductor chip 1 and the size of the bent part 10.

SUMMARY OF THE INVENTION

[0017] Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device and a method of producing the same, in which the problems described above are eliminated.

[0018] Another and more specific object of the present invention is to provide a semiconductor device comprising a semiconductor chip having top and bottom surfaces, upper leads electrically coupled to the semiconductor chip, where a first gap is formed between the upper leads and the top surface of the semiconductor chip, lower leads electrically coupled to the semiconductor chip, where a second gap is formed between the lower leads and the bottom surface of the semiconductor chip, and an encapsulating resin which encapsulates the semiconductor chip so as to maintain the first and second gaps. According to the semiconductor device of the present invention, the leads can be arranged with a large degree of freedom. It is also possible to reduce the size of the semiconductor device by efficiently arranging the leads and reducing the wiring space. In addition, no insulator exclusively for isolating the semiconductor chip and the leads is necessary, thereby making it possible to eliminate the problems which would be generated if the insulator were used.

[0019] Still another object of the present invention is to provide a semiconductor device comprising a stage having top and bottom surfaces, a semiconductor chip which is mounted on the top surface of the stage and having a circuit forming surface, a plurality of leads respectively having inner and outer leads, where each of the inner leads have tip ends which are located above the circuit forming surface of the semiconductor chip and are electrically coupled to the semiconductor chip and a gap is formed between the inner leads and the circuit forming surface of the semiconductor chip, and an encapsulating resin which encapsulates the semiconductor chip and the inner leads so as to maintain the gap and so that the outer leads extend outwardly of the encapsulating resin. According to the semiconductor device of the present invention, it is possible to provide the semiconductor chip on the entire surface of the stage within the encapsulating resin, while isolating the inner leads and the semiconductor chip without the need for an insulator exclusively for the isolation. Hence, it is possible to encapsulate a semiconductor chip which has approximately the same size as the package itself, without deteriorating the reliability of the semiconductor device.

[0020] A further object of the present invention is to provide a method of producing a semiconductor device which includes a semiconductor chip mounted on a stage which is integrally formed on lower leads, upper leads which is separated from the lower leads, and an encapsulating resin which encapsulates the semiconductor chip, comprising the steps of (a) overlapping the upper leads on top of the lower leads via a spacer which is interposed between the upper leads and the stage and has a thickness greater than that of the semiconductor chip, so that a gap is formed between the upper leads and the semiconductor chip, (b) encapsulating the semiconductor chip by the encapsulating resin, and (c) removing the spacer after the step (b). According to the method of the present invention, it is possible to isolate the semiconductor chip and the inner leads without the need for a special process, and the required isolation can be achieved by the resin encapsulation made during the molding process. Therefore, it is possible to produce inexpensive semiconductor devices.

[0021] Another object of the present invention is to provide a method of producing a semiconductor device comprising the steps of (a) mounting a semiconductor chip on a stage, where the semiconductor chip has a circuit forming surface, (b) electrically connecting each of inner leads having tip ends which are located above the circuit forming surface of the semiconductor chip to the semiconductor chip, where the inner leads form leads together with outer leads, and (c) encapsulating the semiconductor chip and the inner leads by an encapsulating resin in a state where a predetermined gap is formed between the inner leads and the circuit forming surface of the semiconductor chip, so that the outer leads extend outwardly of the encapsulating resin. According to the method of the present invention, it is possible to produce highly reliable semiconductor devices at a low cost and without the need for a complex process.

[0022] Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023]

FIG.1 shows an example of a conventional semiconductor device having the COL structure;

FIG.2 shows an example of a conventional semiconductor device having the LOC structure;

FIG.3 shows another examples of the conventional semiconductor device having the LOC structure;
FIG.4 shows a first embodiment of a semiconductor device according to the present invention;
FIG.5 shows lower leads of the first embodiment of the semiconductor device in more detail;
FIG.6 is a perspective view showing the height relationship between the lower leads and a stage;
FIG.7 is a side view showing the height relationship between the lower leads and the stage;
FIG.8 is a plan view showing upper leads of the first embodiment of the semiconductor device in more detail;
FIG.9 is a cross sectional view for explaining a space formed at a sloping part of the stage;
FIG.10 is a cross sectional view showing a second embodiment of the semiconductor device according to the present invention;
FIG.11 is a cross sectional view for explaining a first embodiment of a producing method according to the present invention;
FIG.12 shows a third embodiment of the semiconductor device according to the present invention;
FIG.13 is a plan view showing the semiconductor chip of the third embodiment of the semiconductor device;
FIG.14 shows a stage frame of the third embodiment of the semiconductor device;
FIG.15 shows a lead frame of the third embodiment of the semiconductor device;
FIG.16 is a plan view for explaining a lower die used in a second embodiment of the producing method according to the present invention;
FIG.17 is a diagram for explaining the second embodiment of the producing method;
FIG.18 shows a semicompleted product which is obtained at one stage of the second embodiment of the producing method;
FIG.19 is a diagram for explaining a third embodiment of the producing method according to the present invention;
FIG.20 is a diagram for explaining a fourth embodiment of the producing method according to the present invention;
FIG.21 is a diagram for explaining a wire bonding process which is used in the producing method according to the present invention;
FIGS.22 through 25 show different embodiments of the stage frame;
FIG.26 is a diagram for explaining a process of bending the stage frame;
FIG.27 is a diagram for explaining expansion of stage support parts of the stage frame;
FIG.28 shows an embodiment of a bending part of the stage support part;
FIG.29 shows another embodiment of the bending part of the stage support part;
FIG.30 is a side view for explaining a target value for bending the stage frame;
FIG.31 is a cross sectional view for explaining thicknesses of an encapsulating resin at various parts of the semiconductor device;
FIG.32 is a cross sectional view for explaining an unfilled part formed between the inner leads and the circuit forming surface of the semiconductor chip;
FIG.33 is a cross sectional view for explaining a fifth embodiment of the producing method according to the present invention;
FIG.34 is a diagram showing an essential part of a stage support part used in the fifth embodiment of the method;
FIG.35 is a diagram showing an essential part of another stage support part used in the fifth embodiment of the method;
FIG.36 shows a fourth embodiment of the semiconductor device according to the present invention; and
FIG.37 shows a fifth embodiment of the semiconductor device according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] FIG.4 shows a first embodiment of a semiconductor device according to the present invention. In FIG.4, (A) shows a plan view of the semiconductor device with a part of the encapsulating resin omitted, (B) shows a front view of the semiconductor device with a part of an encapsulating resin omitted, and (C) shows a side view of the semiconductor device viewed from a direction C in (B) with a part of the encapsulating resin omitted.

[0025] In FIG.4, a semiconductor chip 1 is positioned within a space defined by upper leads 11 and lower leads 12, and is mounted on a stage 13 which is formed by a part of the lower leads 12. The semiconductor chip 1 is fixed to the stage 13 by an adhesive agent. The upper leads 11 are approximately parallel to the lower leads 12.

[0026] A circuit forming surface 1a of the semiconductor chip 1 confronts the upper leads 11 with a predetermined gap formed therebetween. On the other hand, a surface of the semiconductor chip 1 on the opposite side of the circuit forming surface 1a confronts the lower leads 12 with a predetermined gap formed therebetween. Electrodes 1b of the semiconductor chip 1 and predetermined ones of the upper and lower leads 11 and 12 are connected via bonding wires 3. The semiconductor chip 1 is encapsulated by an encapsulating resin 2 except for a part of the upper and lower leads 11 and 12. Accordingly, the encapsulating resin 2 fills the gap between the semiconductor chip 1 and the upper leads 11 and the gap between the semiconductor chip 1 and the lower leads 12. In other words, the semiconductor chip 1, the upper leads 11 and the lower leads 12 are

fixed in a mutually isolated state.

[0027] Therefore, according to this embodiment, the leads 11 and 12 are respectively arranged on both sides, that is, the top and bottom surfaces of the semiconductor chip 1. For this reason, the degree of freedom of the circuit design is improved and a more efficient wiring can be made compared to the case where the leads are provided on only one surface of the semiconductor chip.

[0028] In addition, the semiconductor chip 1 is fixed on the stage 13, and the encapsulating resin 2 isolates the semiconductor chip 1 and the upper and lower leads 11 and 12. Hence, there is no need to provide an insulator exclusively for isolating the semiconductor chip 1 from the leads. As a result, this embodiment can prevent the package from cracking due to insufficient adhesion between the insulator and the encapsulating resin.

[0029] Furthermore, this embodiment can be produced by a conventional method of producing the semiconductor device, and no new or special process is required which would otherwise increase the cost of the semiconductor device.

[0030] FIG.5 shows the shape of the lower leads 12 in more detail. In FIG.5, (A) shows a plan view of the lower leads 12, and (B) shows a side view of the lower leads 12. In FIG.5 (A), a two-dot chain line indicates a boundary of the encapsulating resin 2.

[0031] Each of the lower leads 12 and the stage 13 are integrally connected at an outer part before the semiconductor chip 1 is encapsulated by the encapsulating resin 2 to form the semiconductor device. FIG.5 shows a state where the outer part is cut off after encapsulation of the semiconductor chip 1 by the encapsulating resin 2.

[0032] The lower leads 12 have at respective ends thereof top surfaces 12b which connect to the upper leads 11. In addition, a cavity is formed at a central part of the lower leads 12 when viewed as a whole. This cavity is formed by a press, and sloping parts 12a are formed between the top surfaces 12b and the bottom surface of the cavity. Moreover, the stage 13 which is formed by a part of the lower leads 12 is located at an intermediate part between the top surfaces 12b and the bottom surface of the cavity. Sloping parts 13a are formed on the stage 13.

[0033] FIGS.6 and 7 show the height relationship between the stage 13 and the bottom surface of the cavity of the lower leads 12. FIG.6 is a perspective view and FIG.7 is a side view. In FIGS.6 and 7, a two-dot chain line indicates a boundary of the encapsulating resin 2.

[0034] As shown in FIG.7, there is a height difference A between the bottom surface of the cavity of the lower leads 12 and the mounting surface of the stage 13 for receiving the semiconductor chip 1. The encapsulating resin 2 fills this height difference (or space) A, so as to isolate the semiconductor chip 1 and the lower leads 12.

[0035] On the other hand, a distance B shown in FIG.7 from the top surfaces 12b of the lower leads 12 to the stage 13 is greater than the thickness of the semiconductor chip 1. For this reason, when the upper leads 11 are arranged on the top surfaces 12b as shown in FIG.4, a space is formed between the semiconductor chip 1 and the upper leads 11. The encapsulating resin 2 fills this space, so as to isolate the semiconductor chip 1 and the upper leads 11.

[0036] Therefore, the problems such as cracking of the package due to the use of the insulator are eliminated in this embodiment by filling the above spaces by the encapsulating resin 2, without the providing the insulator exclusively for isolation between the semiconductor chip 1 and the upper and lower leads 11 and 12. Accordingly, it is possible to improve the reliability of the semiconductor device.

[0037] FIG.8 shows the shape of the upper leads 11 in more detail. In FIG.8, a two-dot chain line indicates a boundary of the encapsulating resin 2.

[0038] Similarly to the lower leads 12, the upper leads are also integrally connected to an outer part before the encapsulation by the encapsulating resin 2. Each upper lead 11 projecting to the outside of the encapsulating resin 2 has a position and size so as to overlap the corresponding lower lead 12. After the encapsulation by the encapsulating resin 2, each pair of corresponding upper and lower leads 11 and 12 function as a single lead in the overlapped state.

[0039] Because the upper leads 11 and the lower leads 12 are independent parts, it is possible to form a lead part having a desired function using mutually different materials for the upper and lower leads 11 and 12. For example, it is possible to use a copper alloy having a good thermal conductivity for the lower leads 12 because the semiconductor chip 1 which generates heat during operation is mounted on the stage 13 which is formed by the lower leads 12. On the other hand, it is possible to use for the upper leads 11 a steel alloy having a smaller coefficient of expansion than that of the copper alloy since the upper leads 11 are located in the vicinity of the circuit forming surface 1a of the semiconductor chip 1.

[0040] In addition, in this embodiment, the lower leads 12 are used as power source lines 12c, and the upper leads 11 are used as signal lines. The upper leads 11 are arranged near the circuits of the semiconductor chip 1, and a potential difference may cause undesirable effects on the circuits if the upper leads 11 are used as the power source lines. For this reason, the lower leads 12 are used as the power source lines 12c. Furthermore, when the lower leads 11 are used as the power source lines 12c, the wirings of the power source lines within the semiconductor chip 1 can be formed by the lower leads 11, thereby making it possible to reduce the size of the semiconductor chip 1.

[0041] Next, a description will be given of a second embodiment of the semiconductor device according to the present invention, by referring to FIGS.9 through 11. In FIGS.9 through 11, those parts which are the same

as those corresponding parts in FIGS.4 through 8 are designated by the same reference numerals, and a description thereof will be omitted.

[0042] In the first embodiment, the stage 13 is supported in the longitudinal direction of the lower leads 12 as shown in FIG.9. The semiconductor chip 1 is mounted on the stage 13, and the upper leads 11 must be separated from the semiconductor chip 1. Hence, the stage 13 connects to the lower leads 12 via the sloping parts 13a. An inclination angle θ of the sloping part 13a is 45° at the maximum due to the limit of the press forming process. For this reason, a dead space D is formed within the encapsulating resin 2 as shown in FIG.9.

[0043] Accordingly, in the second embodiment, measures are taken so that a larger semiconductor chip can be packaged within the encapsulating resin 2 of the same size.

[0044] In other words, as shown in FIG.10, the stage 13 is connected to a part of the lower leads 12 on the bottom side of the semiconductor chip 1. Hence, the stage 13 does not have sloping parts which extend upwardly, and has a flat shape for the entire surface thereof. Because of this shape of the stage 13, it is sufficient to leave the space for the encapsulating resin 2 on the side of the semiconductor chip 1, and the mounting surface of the semiconductor chip 1 can be increased.

[0045] Next, a description will be given of a first embodiment of a producing method according to the present invention for producing the semiconductor device, by referring to FIG.11. In this embodiment of the producing method, it is assumed for the sake of convenience that the second embodiment of the semiconductor device shown in FIG.10 is produced.

[0046] In FIG.11, the semiconductor chip 1 is first adhered on the stage 13 by silver paste or the like. Then, a spacer 140 which is made of the same material as the leads is placed at a predetermined position on the stage 13, and the upper leads 11 are placed on top of the spacer 140. This spacer 140 has a height which is slightly greater than that of the semiconductor chip 1. Hence, a space is formed between the upper leads 11 and the circuit forming surface 1a of the semiconductor chip 1.

[0047] Thereafter, the stage 13, the spacer 140 and the upper leads 11 are fixed by a laser beam welding or the like, and the semiconductor chip 1 and the upper and lower leads 11 and 12 are bonded. An assembly which is made up of the semiconductor chip 1 and the upper and lower leads 11 and 12 is placed on a lower die of a pair of upper and lower dies used for the encapsulation. In this state, a part of the stage 13 which connect to the lower leads 12 is located at the surface where the upper and lower dies are joined, and the spacer 140 is located above this part of the stage 13. The encapsulating resin 2 is injected into the joined upper and lower dies.

[0048] After the encapsulation by the encapsulating resin 2, the semiconductor device is removed from the upper and lower dies, and a part of the spacer 140 projecting from the encapsulating resin 2 is cut and removed by a press or the like. Hence, the lower leads 12 shown in FIG.10 are formed.

[0049] According to this embodiment of the producing method, the spacer 140 is used to separate the semiconductor chip 1 and the upper leads 11 during the production process. As a result, it is possible to eliminate the sloping parts 13a which extend upwardly from the stage 13. Consequently, the space for arranging the semiconductor chip 1 within the encapsulating resin 2 is increased, and a larger semiconductor chip can be encapsulated within the encapsulating resin 2 of the same size when compared to the first embodiment of the semiconductor device.

[0050] Next, a description will be given of a third embodiment of the semiconductor device according to the present invention, by referring to FIG.12. In FIG.12, (A) shows a front view of the semiconductor device with a part shown in cross section, and (B) shows a side view of the semiconductor device with a part shown in cross section.

[0051] A semiconductor device 14 shown in FIG.12 has a MF-LOC (Multi Frame-Lead on Chip) structure. That is, a semiconductor chip 1 is mounted on a stage 13, and inner leads 4 are arranged above the semiconductor chip 1 and separated from the semiconductor chip 1. The semiconductor chip 1 and the inner leads 4 are encapsulated by an encapsulating resin 2. The stage 13 is approximately parallel to the inner leads 4.

[0052] The stage 13 has an approximate rectangular plate shape, and includes two stage support parts 130a which project to the left in FIG.12 (A) and two stage support parts 130b which project to the right in FIG.12 (A). Tip ends of the stage support parts 130a and 130b are exposed from the encapsulating resin 2. The semiconductor chip 1 which is fixed on the stage 13 has an approximate rectangular shape which is slightly smaller than that of the stage 13. Circuits are formed on a circuit forming surface 1a of the semiconductor chip 1.

[0053] The inner leads 4 are arranged at constant intervals above the circuit forming surface 1a of the semiconductor chip 1 and separated from the circuit forming surface 1a. Each inner lead 4 is electrically connected to the semiconductor chip 1 via a bonding wire 3.

[0054] As shown in FIG.12 (A), the distance between the stage 13 and each of the inner leads 4 is approximately constant. In addition, the distance between the circuit forming surface 1a and each of the inner leads 4 is also approximately constant. On the other hand, as shown in FIG.12 (A) and (B), each inner lead 4 extends from the central part above the semiconductor chip 1 in an approximately parallel manner to the stage 13 and to the circuit forming surface 1a, and a part of this inner lead 4 which extends outside the encapsulating resin 2 becomes an outer lead 5.

[0055] When the semiconductor device 14 is viewed from outside the encapsulating resin 2, there is a gap between a surface 5a of each outer lead 5 confronting the circuit forming surface 1a and surfaces 130c and 130d of the stage support parts 130a and 130b on the same side as the surface of the stage 13 on which the semiconductor chip 1 is mounted. The surfaces 5a, 130c and 130d are exposed from the encapsulating resin 2, and the gap is the sum of the thickness of the semiconductor chip 1 and the distance between the circuit forming surface 1a and the inner leads 4 along a direction perpendicular to the circuit forming surface 1a.

[0056] The outer leads 5 are respectively bent downwardly in FIG.12 (B) approximately at right angles outside the encapsulating resin 2 to form a J-shape. The semiconductor chip 1 is electrically connected to an external circuit (not shown) by connecting the outer leads 5 to the external circuit.

[0057] Next, a description will be given of a second embodiment of the producing method according to the present invention, by referring to FIGS.13 through 18. In this embodiment of the producing method, it is assumed for the sake of convenience that the third embodiment of the semiconductor device 14 shown in FIG.12 is produced.

[0058] FIGS.13 through 15 respectively show the elements forming the semiconductor device 14. FIG.13 is a plan view of the semiconductor chip 1, FIG.14 shows a stage frame, and FIG.15 shows a lead frame. In FIGS.13 and 14, (A) shows a plan view, (B) shows a front view, and (C) shows a side view.

[0059] As shown in FIG.13, a plurality of bonding pads 7 are provided at a predetermined central part on the circuit forming surface 1a of the semiconductor chip 1. The number of bonding pads 7 corresponds to the number of terminals of the semiconductor device 14, that is, the number of outer leads 5.

[0060] In addition, as shown in FIG.14, a stage frame 9 is made up of a frame 15_1, and the rectangular stage 13 which is connected to the frame 15_1 via the stage support parts 130a and 130b and on which the semiconductor chip 1 is mounted. The size of the stage 13 is slightly larger than that of the semiconductor chip 1, in both the vertical and horizontal directions.

[0061] The stage support parts 130a and 130b respectively include bending parts 10 which project from the stage 13 and is thereafter bent upwardly in FIG.14 (B). The bending parts 10 are further bent to match the plane of the frame 15_1 and connect to the frame 15_1. Accordingly, the top surface of the stage 13 is separated by a distance d from the top surface of the frame 15. This distance d is set greater than the thickness of the semiconductor chip 1.

[0062] A plurality of positioning holes 16 are formed in the frame 15_1, and are used to position the frame 16 during the production process. Some of the positioning holes 16 have an oval shape, while the remaining positioning holes 16 have a circular shape. The oval shaped positioning hole 16 is provided to absorb the expansion and contraction of the frame 15_1 during the production process. Hence, although only four positioning holes 16 are shown in FIG.14 (A) and one of the four positioning holes 16 has the oval shape, a plurality of oval shaped positioning holes 16 are actually arranged at predetermined intervals, for example. Furthermore, the oval shaped positioning holes 16 may be arranged along only one side of the frame 15_1 or along both sides of the frame 15.

[0063] As shown in FIG.15, a lead frame 8 has a plate shape, and the inner leads 4 and the outer leads which extend from the inner leads 4 are respectively connected to a frame 15_2 via connecting parts 18. The lead frame 8 is die cut to a shape such that the tip ends of the inner leads 4 are positioned to facilitate the wire bonding relative to the positions of the bonding pads 7 of the semiconductor chip 1.

[0064] Positioning holes 16 are also formed in the frame 15_2 for the same reasons as the positioning holes 16 formed in the frame 15_1. Furthermore, the positioning holes 16 of the frame 15_2 and the positioning holes 16 of the frame 15_1 are located at corresponding positions to enable accurate positioning relative to each other.

[0065] The semiconductor chip 1 is fixed on the top surface of the stage 13 of the stage frame 9, and the lead frame 8 is placed on top of the stage frame 9 by aligning the two frames via the positioning holes 16. Thereafter, the inner leads 4 and the semiconductor chip 1 are wire bonded by a wire bonding process.

[0066] Next, a description will be given of dies used in the second embodiment of the producing method, and the lower die in particular with reference to FIG.16. In FIG.16, positioning pins 17 penetrate the corresponding positioning holes 16 of the lead frame 8 and the stage frame 9, so as to align each frame and the dies. The frames 15_1 and 15_2 are shown as one frame 15 in FIG.16.

[0067] A lower die 23 generally includes parts having three different depths as indicated by the different hatchings. An upper die (not shown) has a shape corresponding to this shape of the lower die 23.

[0068] The lower die 23 includes a rectangular package part 25a having the largest depth, four support parts 19 projecting up and down in FIG.16 from the package part 25a and having a depth next largest to the package part 25a, a gate part 21 extending down from the center of the package part 25a and having the same depth as the support parts 19, and a rectangular frame shaped lead part 20 surrounding the package part 25a and having the smallest depth.

[0069] The size of the package part 25 in the horizontal and vertical directions is slightly larger than the size of the stage 13 in the horizontal and vertical directions. Two support parts 19 project up from the package part 25a and two support parts 19 project down from the package part 25a in FIG.16, and respectively extend to

the ends of the frame 15. The gate part 21 extends down in FIG.16 and connects to a runner part 22 which extends horizontally along the longitudinal direction of the frame 15. This runner part 22 has the same depth as the gate part 21.

[0070] The lead frame 8 shown in FIG.15 and the stage frame 9 shown in FIG.14 are integrally stacked, and is placed on the lower die 23 in a state where the positioning pins 17 of the lower die 23 penetrate the corresponding positioning holes 16 of the frames 15_1 and 15_2. The encapsulation by the encapsulating resin 2 is made in this state.

[0071] Next, the second embodiment of the producing method will be described in more detail with reference to FIGS.17. FIG.17 shows a state where the stacked lead frame 8 and stage frame 9 are placed on the lower die 23 and an upper die 24 is positioned on top of the lower die 23. In FIG.17, (C) shows a plan view, (A) shows a cross section along a line I-I in (C), (B) shows a cross section along a line II-II in (C), and (D) shows a cross section along a line III-III in (C).

[0072] In FIG.17, the upper die 24 is shaped so as to hold the outer leads 5 of the lead frame 8 which project from the package part 25a and the stage frame 9 which has the stage support parts 130a and 130b at predetermined positions in cooperation with the lower die 23. In other words, the upper die 24 includes a package part 25b which has the same shape as the package part 25a of the lower die 23 at a position corresponding to the package part 25a, flat parts 26 which support the frames 15_2 and 15_1 of the lead frame 8 and the support frame 9, and projecting parts 27 which support the stage support parts 130a and 130b together with the support parts 19 of the lower die 23.

[0073] Thereafter, the encapsulating resin 2 is injected from the runner part 22 via the gate part 21, so as to form a semicompleted product 14a of the semiconductor device 14 as shown in FIG.18. In FIG.18, (A) shows a front view of the semicompleted product 14a with a part of the encapsulating resin 2 omitted, and (B) shows a side view of the semicompleted product 14a with a part of the encapsulating resin 2 omitted.

[0074] The stage support parts 130a and 130b of the semicompleted product 14a shown in FIG.18 is cut at positions indicated by a one-dot chain line in FIG.18 (A), so as to cut the outer leads 5 to predetermined lengths. In addition, the connecting parts 18 shown in FIG.15 are cut to separate each of the outer leads 5. The outer leads 5 are then formed into predetermined shapes so as to make the semiconductor device 14 shown in FIG.12.

[0075] Therefore, according to this embodiment of the producing method, the semiconductor device 14 which is produced has the semiconductor chip 1 mounted on the entire surface of the flat stage 13 which is provided within the encapsulating resin 2. For this reason, it is possible to encapsulate the semiconductor chip 1 which is slightly smaller than the encapsulating resin 2 and larger than the semiconductor chip which could conventionally be encapsulated by the encapsulating resin of the same size. As a result, the size of the package can be reduced according to this embodiment.

[0076] In addition, the inner leads 4 and the circuit forming circuit 1a of the semiconductor chip 1 are isolated by the encapsulating resin 2, and no insulator is provided therebetween exclusively for the isolation. Accordingly, the reliability of the semiconductor device 14 is high in that no mechanical problems are generated which conventionally occurred due to the provision of the insulator.

[0077] Next, a description will be given of a third embodiment of the producing method according to the present invention, by referring to FIG.19. In this embodiment of the producing method, it is assumed for the sake of convenience that the third embodiment of the semiconductor device 14 shown in FIG.12 is produced. In FIG.19, (A) shows a plan view, (B) shows a cross sectional view along a line IV-IV in (A), (C) shows a cross sectional view along a line V-V in (A).

[0078] In FIG.19, a stage frame 9a has the semiconductor chip 1 fixed on the stage 13 thereof, and a spacer 30 indicated by a hatching is placed on the frame 15_1 of the stage frame 9a. This spacer 30 has the same width as the frame 15_1. The frame 15_2 of the lead frame 8 is positioned on the spacer 30 in alignment with the frame 15_1. The frames 15_1 and 15_2 and the spacer 30 are held the upper and lower dies 24a and 23a in the state shown.

[0079] The cross sectional shape of the spacer 30 is rectangular, and the thickness of the spacer 30 is greater than that of the semiconductor chip 1. Hence, the inner leads 4 are separated from the circuit forming surface 1a of the semiconductor chip 1. The coefficient of linear expansion of the spacer 30 is set approximately the same as those of the lead frame 8 and the stage frame 9a.

[0080] In the plan view, the stage frame 9a has a shape similar to that of the stage frame 9 shown in FIG.14. However, the stage frame 9a has a plate shape and does not have the bending parts in support parts 130e and 130f thereof. Positioning holes 16a are formed in the stage frame 9a at positions corresponding to the positioning holes 16 in the lead frame 8. Positioning holes 16b are also formed in the spacer 30 at positions corresponding to the positioning holes 16 and 16a.

[0081] The lower die 23a includes flat parts 31 for making contact with and supporting the frame 15_1 of the stage frame 9a, a package part 25a which has a depth sufficient to encapsulate the semiconductor chip 1 by the encapsulating resin 2, a projecting part 32 for making contact with and supporting the projecting parts 15a and 15b which project from the frame 15_2 of the lead frame 8 as shown in FIG.15, a projecting part 33 which forms a gate part 21a, and a runner part 22a which connects to the gate part 21a.

[0082] The upper die 24a includes flat parts 34 which

make contact with the frame 15_2 of the lead frame 8, projecting parts 35 for making contact with the stage support parts 130e and 130f of the stage frame 9a from above, a package part 25b which has a depth sufficient to encapsulate the semiconductor chip 1 by the encapsulating resin 2, and a shallow connecting part 36 which connects the gate part 21a and the runner part 22a.

[0083] Thereafter, the encapsulating resin 2 is injected from the runner part 22a via the gate part 21, so as to form the semicompleted product 14a of the semiconductor device 14 as shown in FIG.18, similarly to the second embodiment of the producing method.

[0084] According to this third embodiment of the producing method, it is possible to simplify the production process because it is unnecessary to bend the stage frame 9a. In addition, the shapes of the upper and lower dies 24a and 23a are more simple compared to those of the upper and lower dies 24 and 23 used in the second embodiment of the producing method, thereby making it possible to reduce the cost of the upper and lower dies 24a and 23a.

[0085] Next, a description will be given of a fourth embodiment of the producing method according to the present invention, by referring to FIG.20. In this embodiment of the producing method, it is assumed for the sake of convenience that the third embodiment of the semiconductor device 14 shown in FIG.12 is produced. In FIG.20, (A) shows a plan view, (B) shows a cross sectional view along a line VI-VI in (A), (C) shows a cross sectional view along a line VII-VII in (A). In FIG.20, those parts which are the same as those corresponding parts in FIG.19 are designated by the same reference numerals, and a description thereof will be omitted.

[0086] In FIG.20, a spacer 30a includes positioning holes 16c. The positioning holes 16c are located at positions corresponding to the positioning holes 16 and 16a of the lead frame 8 and the stage frame 9a.

[0087] As shown in FIG.20, the stage frame 9a, the spacer 30a and the lead frame 8 are aligned and placed on top of one another, and are held in this state by upper and lower dies 24b and 23b. The cross sectional shape of the spacer 30a is rectangular, and the thickness of the spacer 30a is greater than that of the semiconductor chip 1. Hence, the inner leads 4 of the lead frame 8 are separated from the circuit forming surface 1a of the semiconductor chip 1.

[0088] The coefficient of linear expansion of the spacer 30a is set approximately equal to those of the lead frame 8 and the stage frame 9a, similarly as in the case of the spacer 30 shown in FIG.19.

[0089] The lower die 23b includes flat parts 41 for making contact with and supporting the frame 15_1 of the stage frame 9a, a package part 25a which has a depth sufficient to encapsulate the semiconductor chip 1 by the encapsulating resin 2, and a runner part 22b which connects to a gate part 21b.

[0090] On the other hand, the upper die 24b includes flat parts 42 which make contact with the frame 15_2 of the lead frame 8, a package part 25b which has a depth sufficient to encapsulate the semiconductor chip 1 by the encapsulating resin 2, and the shallow gate part 21b which connects to the runner part 22b.

[0091] A continuous surface is formed by a side surface 25d of the package part 25b of the upper die 24b, a side surface 30b of the spacer 30a on the side of the semiconductor chip 1, and a side surface 25c of the package part 25a of the lower die 23b.

[0092] The encapsulating resin 2 is injected from the runner part 22a via the gate part 21, so as to form the semicompleted product 14a of the semiconductor device 14 as shown in FIG.18, similarly to the second and third embodiments of the producing method.

[0093] According to this fourth embodiment of the producing method, it is possible to simplify the production process because it is unnecessary to bend the stage frame 9a. In addition, the shapes of the upper and lower dies 24b and 23b are more simple compared to those of the upper and lower dies 24a and 23a used in the third embodiment of the producing method, thereby making it possible to further reduce the cost of the upper and lower dies 24b and 23b.

[0094] Next, a description will be given of a bonding process of the producing method. According to the second through fourth embodiments of the producing method, the circuit forming surface 1a of the semiconductor chip 1 and the inner leads 4 are separated in the state where the lead frame 8 and the stage frame 9 or 9a are stacked, and the inner leads 4 are wire bonded to the semiconductor chip 1 in this state.

[0095] Accordingly, if the conventional wire bonding technique using ultrasonic waves is employed, it is difficult to positively make the wire bonding because the bonding parts of the inner leads 4 vibrate. Hence, in the present invention, it is possible to make a more reliable wire bonding by taking the following measures.

[0096] FIG.21 is a diagram for explaining the wire bonding process. In FIG.21, (A) generally shows a wire bonder, and (B) and (C) respectively explain the bonding process.

[0097] In FIG.21 (A), the semiconductor chip 1 which is to be wire bonded is placed on the stage 13 of the stage frame 9, and the inner leads 4 of the lead frame 8 are arranged above the semiconductor chip 1 so that a gap is formed between the circuit forming surface 1a of the semiconductor chip 1 and the inner leads 4. Shock absorbing members 100 are arranged on the tip end bottom surfaces of the inner leads 4 confronting the circuit forming surface 1a.

[0098] A plurality of bonding pads 7 made of aluminum electrodes are arranged at a central part on the circuit forming surface 1a of the semiconductor chip 1. The lead frame 8 and the stage frame 9 are stacked and placed on a heater 103.

[0099] A capillary 101 which forms a part of the wire bonder is positioned above the semiconductor chip 1. A hole having a diameter slightly greater than the diame-

ter of the bonding wire is formed in the capillary 101. The bonding wire is inserted through this hole of the capillary 101 and is supplied under guidance thereby. The capillary 101 is mounted on a transducer (not shown). The transducer vibrates due to ultrasonic oscillation, and connects the bonding wire by ultrasonic bonding.

[0100] A frame holder 102 which also forms a part of the wire bonder is arranged above the inner leads 4. As shown in FIG.21 (A), the frame holder 102 has L-shaped tip ends, and each tip end is pivottable in directions A and B.

[0101] As shown in FIG.21 (B), an appropriate weight is applied on top of the inner leads 4 by pivotting the tip ends of the frame holder 102 in the direction A, so that the shock absorbing members 100 make contact with the circuit forming surface 1a of the semiconductor chip 1. The weight applied on top of the inner leads 4 is not excessively large so as to prevent the circuit forming surface 1a from becoming damaged. In addition, the weight applied on top of the inner leads 4 is sufficiently large so that the tip ends of the inner leads 4 to which the bonding wires 3 are connected make contact with the circuit forming surface 1a and is mechanically stable to enable stable ultrasonic bonding.

[0102] The bonding wire 3 is guided by the capillary 101 in the state where the shock absorbing members 100 make contact with the circuit forming surface 1a by the action of the frame holder 102. And, the wire bonding is made so that the bonding wire 3 connects a predetermined inner lead 4 to the corresponding bonding pad 7.

[0103] When the wire bonding is completed for all of the inner leads 4, the tip ends of the frame holder 102 pivot in the direction B, and the weight applied on the inner leads 4 is released. As a result, the inner leads 4 return to their original state by the resiliency thereof, and the inner leads 4 become parallel to the circuit forming surface 1a. In this state, the gap is formed between the inner leads 4 and the circuit forming surface 1a as shown in FIG.21 (C).

[0104] By bonding the semiconductor chip 1 and the inner leads 4 in the above described manner, it becomes possible to make a highly reliable wire bonding with respect to the semiconductor device having the LOC structure such that the gap is formed between the semiconductor chip and the inner leads. Thereafter, the resin encapsulation by the encapsulating resin 2 is made by any of the methods described above with reference to FIGS.16 through 20, and the semiconductor device having the same configuration as that shown in FIG.12 is completed. In this completed semiconductor device, the shock absorbing members 100 are provided on the inner leads 4 and separated from the circuit forming surface 1a of the semiconductor chip 1.

[0105] The stage frame 9 releases the heat generated from the semiconductor chip 1 to the outside. But because the metal stage frame 9 and the encapsulating resin 2 make contact, a crack may be formed in the package, that is, the encapsulating resin 2, due to the difference in the coefficients of expansion. For this reason, it is desirable to minimize the area of contact between the stage frame 9 and the encapsulating resin 2 in order to prevent cracking of the encapsulating resin 2.

[0106] Next, a description will be given of embodiments of the stage frame which are designed to minimize the area of contact between the stage frame and the encapsulating resin, by referring to FIGS.22 through 25. In FIGS.22 through 25, (A) shows a plan view, (B) shows a front view, and (C) shows a side view.

[0107] In a stage frame 50 shown in FIG.22, stages 51b and 51a for respectively supporting right and left end parts of the semiconductor chip 1 are connected to and supported on the frame 15 via stage supports 52b and 52a which have bending parts.

[0108] In a stage frame 53 shown in FIG.23, two rod support parts 54a and 54b which respectively have bending parts on the right and left ends thereof are connected to the frame 15. The semiconductor chip 1 is supported along the horizontal direction in FIG.23 (A) by these two rod support parts 54a and 54b.

[0109] In a stage frame 55 shown in FIG.24, a stage 56 supports the central part of the semiconductor chip 1 along the horizontal direction in FIG.24 (A). The stage 56 connect to T-shaped parts 57a and 57b, and the T-shaped parts 57a and 57b further connect to the frame 15 via stage support parts 52a and 52b.

[0110] In a stage frame 58 shown in FIG.25, a stage 59 supports the central part of the semiconductor chip 1 along the vertical direction in FIG.25 (A). Both ends of the stage 59 are connected to the frame 15 via stage support parts 52c and 52d.

[0111] According to the stage 56 of the stage frame 55, it is possible to effectively support the weight on the semiconductor chip 1 during the bonding process if the bonding pads on the semiconductor chip 1 are arranged in the horizontal direction in FIG.24 (A).

[0112] On the other hand, according to the stage 59 of the stage frame 58, it is possible to effectively support the weight on the semiconductor chip 1 during the bonding process if the bonding pads on the semiconductor chip 1 are arranged in the vertical direction in FIG.25 (A).

[0113] According to the stage frames 50, 53, 55 and 58, stepped parts (or differences in heights) are formed between the frame 15 and the stages 51a, 51b, 56 and 59 and the support parts 54a and 54b by the provision of the bending parts. The distances between the top surface of the frame 15 and the top surfaces of the stages 51a, 51b, 56 and 59 and the support parts 54a and 54b in the vertical direction in (B) of FIGS.22 through 25 are respectively greater than the thickness of the semiconductor chip 1.

[0114] Therefore, when the semiconductor chip 1 is placed on any of the stages 51a, 51b, 56 and 59 and the

support parts 54a and 54b and the lead frame 8 (not shown) is placed thereon, the circuit forming surface 1a of the semiconductor chip 1 becomes separated from the lead frame 8, thereby maintaining the insulation between the lead frame 8 and the semiconductor chip 1.

[0115] The gap is formed between the circuit forming surface 1a of the semiconductor chip 1 and the lead frame 8, regardless of which one of the stage frames described above is used. Hence, the semiconductor device which is obtained can positively encapsulate by the encapsulating resin 2 a semiconductor chip which is only slightly smaller than the package, similarly to the semiconductor device 14. As a result, it is possible to realize a semiconductor device having the MF-LOC structure such that the size of the package is reduced to approximately the size of the semiconductor chip encapsulated therein.

[0116] Next, a description will be given of the process of bending the stage support parts 130a and 130b of the stage frame 9 shown in FIG.14. As shown in FIG.26, the stage frame 9 is placed on a lower base 101 of a press and is fixed at a part P, and an upper part 102 is moved down in a direction X so as to bend the stage frame 9 as indicated by a dotted line.

[0117] However, although the stage support part 130a, for example, has a length a as shown in FIG.27 (A) before being press formed, the stage support part 130a has an expanded length a' (a' > a) after the bending as shown in FIG.27 (B). If the thickness of the stage frame 9 is denoted by t, the limit of the bending is such that t' = 1.5t to 2.0t. If the bending exceeds this limit and t' becomes greater than 2.0t, the stage frame 9 may break at the stage support part 130a.

[0118] Hence, in the third embodiment of the semiconductor device, the stage support parts 130a and 130b are provided with the bending parts 10. The bending parts 10 facilitate the bending of the stage support parts 130a and 130b, and help prevent breaking of the stage support parts 130a and 130b during the bending process of the stage frame 9.

[0119] FIG.28 shows an embodiment of the bending part 10. In FIG.28, (A) shows a plan view, and (B) shows a side view. In this embodiment, the bending part 10 has a reduced width compared to the remaining parts of the stage support part 130a, so as to facilitate the bending of the stage support part 130a. For example, this bending part 10 may be formed by partially etching a part of the stage support part 130a.

[0120] FIG.29 shows another embodiment of the bending part 10. In FIG.29, (A) shows a plan view, and (B) shows a side view. In this embodiment, the bending part 10 has a reduced width and a reduced thickness compared to the remaining parts of the stage support part 130a, so as to facilitate the bending of the stage support part 130a. For example, this bending part 10 may be formed by partially etching a part of the stage support part 130a or press forming the reduced thickness part.

[0121] According to the third embodiment of the semiconductor device, for example, the gap between the inner leads 4 and the circuit forming surface 1a of the semiconductor chip 1 is determined by the precision with which the cavity or space is formed in the stage frame 9 to accommodate the semiconductor chip 1. Hence, when bending the stage frame 9, the tolerance of this gap must be taken into consideration.

[0122] However, although the bending which takes the tolerance into consideration may be realized when the thickness of the package is relatively large, it becomes extremely difficult to accurately bend the stage frame 9 while taking the tolerance into consideration if the thickness of the package is small. In the latter case, the space between the stage frame 9 and the inner leads 4 cannot be formed accurately. As a result, the gap between the inner leads 4 and the circuit forming surface 1a cannot be formed accurately, and the encapsulating resin 2 cannot satisfactorily fill the gap between the inner leads 4 and the circuit forming surface 1a if the gap becomes too narrow. If the encapsulating resin 2 cannot fully fill the gap, the reliability of the semiconductor device greatly deteriorates.

[0123] FIG.30 shows a target value La for the space between the stage frame 9 and the inner leads 4. For example, the stage frame 9 can be bent to the target value La $\pm$ 0.1 mm. On the other hand, FIG.31 shows a cross section of the semiconductor device. The encapsulating resin 2 above the inner leads 4 has a thickness Lc, and the encapsulating resin 2 between the inner leads 4 and the circuit forming surface 1a of the semiconductor chip 1 is Lb. Hence, if the target value La has the error of $\pm$0.1 mm, the thickness Lb may vary in a range of $\pm$0.1 mm. If the thickness Lc can be reduced so that the thickness Lb can be increased without increasing the overall width of the semiconductor device, it is possible to substantially neglect the error of $\pm$0.1 mm which may occur in the thickness Lb. However, when the overall thickness of the semiconductor device is relatively small, the thickness Lc cannot be reduced and it is therefore impossible to increase the thickness Lb.

[0124] The present inventor has found that when the thickness Lb < 0.1 mm, the encapsulating resin 2 may not satisfactorily fill the gap between the inner leads 4 and the circuit forming surface 1a of the semiconductor chip 1 as shown in FIG.32. As a result, an unfilled part 200 is formed between the inner leads 4 and the circuit forming surface 1a. In this case, the reliability of the semiconductor device greatly deteriorates due to the insufficient isolation between the inner leads 4 and the circuit forming surface 1a.

[0125] Next, a description will be given of a fifth embodiment of the producing method according to the present invention, by referring to FIG.33.

[0126] This embodiment of the producing method utilizes the precision of the upper and lower dies 24 and 23 which are used when encapsulating the semiconductor chip 1 by the encapsulating resin 2. In other words,

when the upper and lower dies 24 and 23 are fit together prior to injecting the encapsulating resin 2 therein, the upper and lower dies 24 and 23 forcibly correct the target value La, particularly by the pressing action at the parts indicated by the arrows. At the part indicated by the arrows on the left side, the spacer 140 and the lower die 23 cooperate to correct the target value La. This spacer 140 also functions similarly to the spacer 140 of the embodiment shown in FIG.11.

[0127] As a result, the tolerance of the target value La is corrected to La ± 0.2 mm to La ± 0.3 mm regardless of the size of the error introduced at the time of bending the stage frame 9 as shown in FIG.30. For this reason, this embodiment of the producing method can guarantee the gap between the inner leads 4 and the circuit forming surface 1a of the semiconductor device 1, that is, the thickness Lb shown in FIG.31, to the designed value. In other words, the formation of the unfilled part 200 shown in FIG.32 is positively prevented.

[0128] FIGS.34 and 35 show embodiments of the bending part 10 of the stage support part 130a (and 130b) for facilitating the correction of the target value La by the upper and lower dies 24 and 23. In FIGS.34 and 35, (A) shows a plan view, and (B) shows a side view.

[0129] In FIG.34, the bending part 10 has a generally inverted U-shape. On the other hand, the bending part 10 shown in FIG.35 has a zigzag shape. These shapes of the bending part 10 facilitate the correction of the target value La because slight expansion or contraction can be absorbed thereby.

[0130] Next, a description will be given of a fourth embodiment of the semiconductor device according to the present invention, by referring to FIG.36. In FIG.36, those parts which are the same as those corresponding parts in FIGS.12 through 15 are designated by the same reference numerals, and a description thereof will be omitted. In FIG.36, (A) shows a partial plan view, and (B) shows a partial cross sectional view.

[0131] As indicated by an encircled part Y in FIG.36 (A), the inner lead 4 and the stage support part 130a intersect in the plan view. This intersection in the plan view is made possible because two frames 15_1 and 15_2, that is, the stage frame 9 and the lead frame 8, are stacked and aligned using the positioning holes 16 at parts which do not remain as the package. Because this intersection in the plan view is made possible, this embodiment of the semiconductor device has an additional advantage in that the freedom of design of the inner leads 4 is increased. In other words, the inner leads 4 can be designed with more degree of freedom compared to the case where the above intersection in the plan view is impossible

[0132] Next, a description will be given of a fifth embodiment of the semiconductor device according to the present invention, by referring to FIG.37. In FIG.37, (A) shows a front view of the semiconductor device with a part shown in cross section, and (B) shows a side view of the semiconductor device with a part shown in cross section. In FIG.37, those parts which are the same as those corresponding parts in FIG.12 are designated by the same reference numerals, and a description thereof will be omitted.

[0133] In this embodiment, the bottom surface of the stage 13 is exposed from the encapsulating resin 2. In other words, no encapsulating resin 2 is formed on the bottom surface of the stage 13. As a result, the stage 13 itself acts as a radiator for efficiently radiating the heat which is generated from the semiconductor chip 1 during operation. In addition, the elimination of the encapsulating resin 2 on the bottom surface of the stage 13 efficiently reduces the thickness of the semiconductor device (package), even though two frames 15_1 and 15_2, that is, the stage frame 9 and the lead frame 8, are used.

[0134] Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A semiconductor device, comprising

   a semiconductor chip (1) having top and bottom surfaces, and
   upper leads (11) electrically coupled to said semiconductor chip (1),
   a first gap being formed between said upper leads (11) and the top surface (1a) of said semiconductor chip (1), and
   an encapsulating resin (2) which encapsulates said semiconductor chip (1) and fills said first gap,
   characterized in that
   lower leads (12) are provided, being electrically coupled to said semiconductor chip (1),
   a stage (13) is provided on which said semiconductor chip (1) is mounted, and
   a second gap is formed between said lower leads (11) and said bottom surface of said semiconductor chip (1), said encapsulating resin (2) also filling said second gap completely.

2. A semiconductor device according to claim 1, **characterized in that**

   said stage has a different height position compared to a height position of said lower leads (12) so as to maintain said second gap, said stage being encapsulated by said encapsulating resin (2).

3. A semiconductor device according to claim 1 or 2, **charaterized in that**

said upper leads (11) input or output signals to said semiconductor chip (1) and said lower leads (12) supply a power supply voltage.

4. A semiconductor device according to any of claims 1 to 3, **characterized in that**

said upper leads (11) and said lower leads (12) are made of mutually different materials.

5. A semiconductor device according to any of claims 1 to 4, **characterized in that**

said upper leads (11) and said lower leads (12) are approximately parallel to each other within said encapsulating resin (2) when viewed in a cross section of said encapsulating resin (2).

6. A method of producing a semiconductor device which includes a semiconductor chip (1) mounted on a stage (13) which is integrally formed on lower leads (12), upper leads (11) being separated from said lower leads, and an encapsulating resin (2) which encapsulates said semiconductor chip (1), **characterized by the steps of**

(a) overlapping said upper leads (11) on top of said lower leads (12) via a spacer (140) which is interposed between said lower leads and said stage and has a thickness greater than that of said semiconductor chip (1), so that a gap is formed between said upper leads (12) and said semiconductor chip (1);
(b) encapsulating said semiconductor chip (1) by said encapsulating resin (2); and
(c) removing said spacer (140) after said step (b).

7. A method according to claim 6, **characterized in that**

different materials are used for said upper leads (11) and said lower leads (12).

8. A method according to claim 6 or 7, **characterized in that**

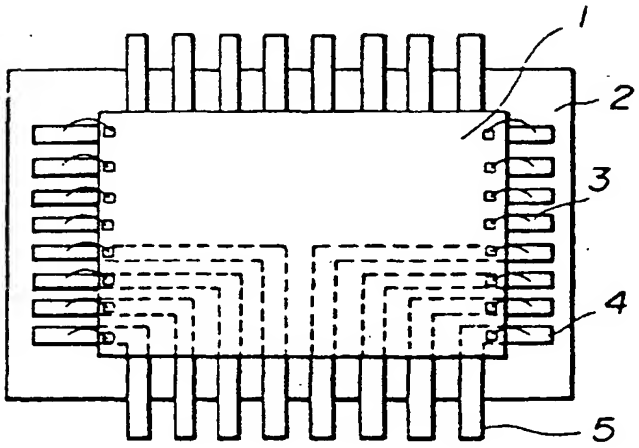
said step (a) overlaps said upper leads (11) on top of said lower leads (12) via said spacer (140) so that said upper leads (11) are approximately parallel to said lower leads (12) within said encapsulating resin (2) when viewed in a cross section of said encapsulating resin (2).

9. A method according to claim 8, **characterized in that**

said step (a) overlaps said upper leads (11) on top of said lower leads (12) via said spacer (140) so that said upper leads (11) and said lower leads (12) make contact outside said encapsulating resin (2).

FIG. 1 PRIOR ART

(A)



(B)

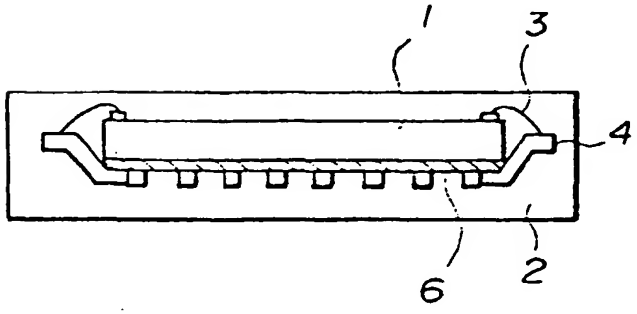
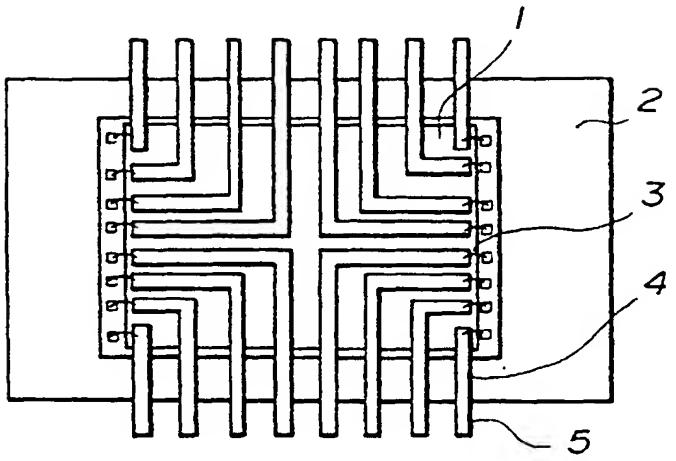


FIG.2 PRIOR ART

(A)



(B)

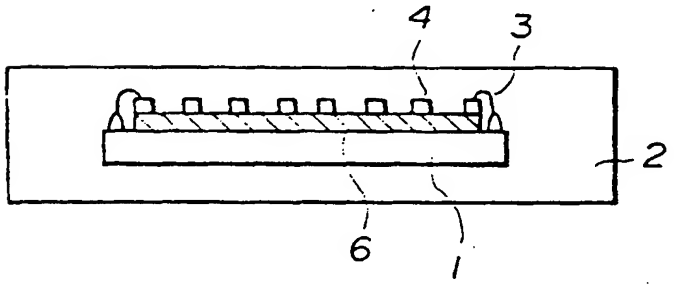


FIG.3 PRIOR ART

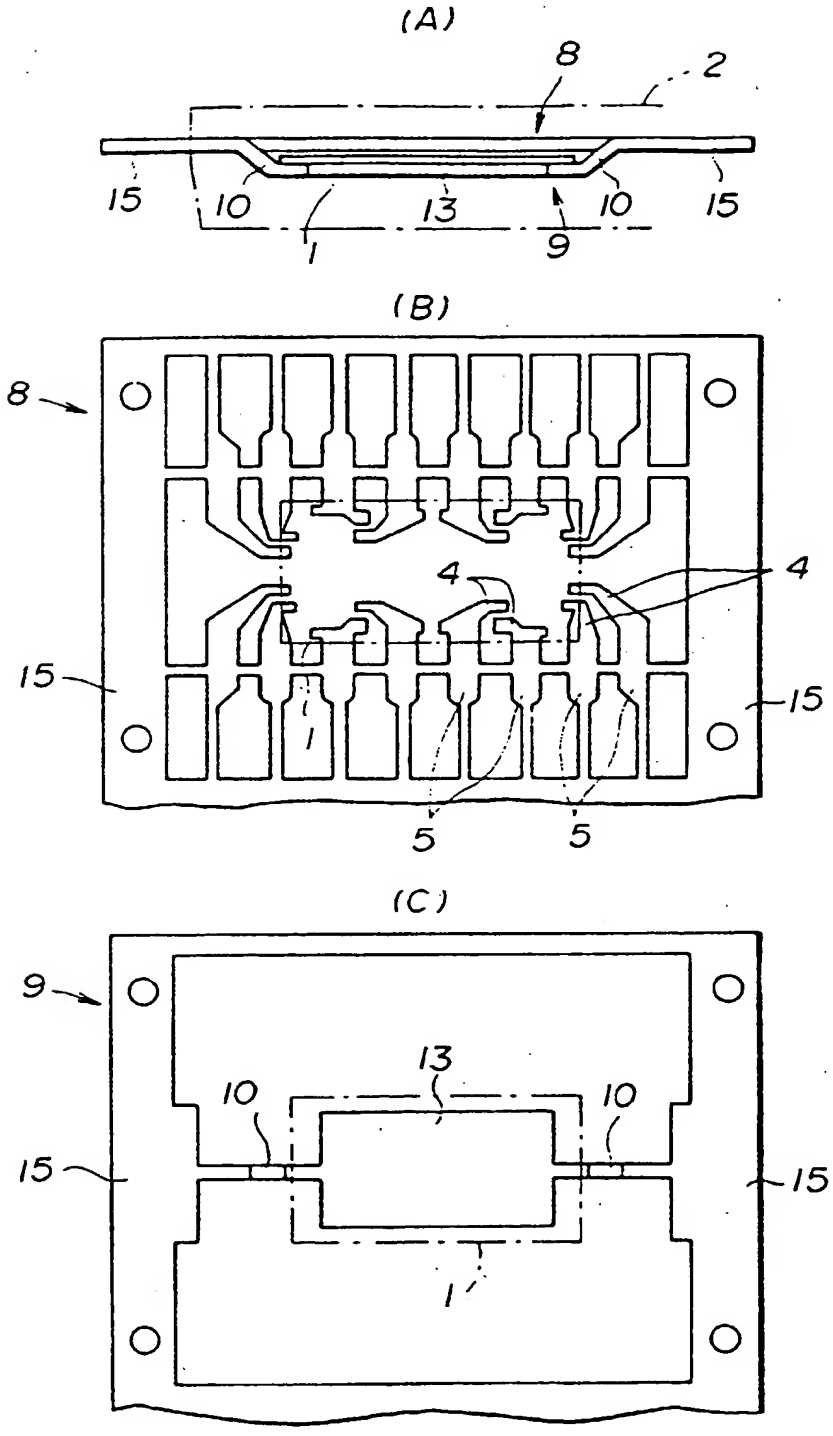


FIG.4

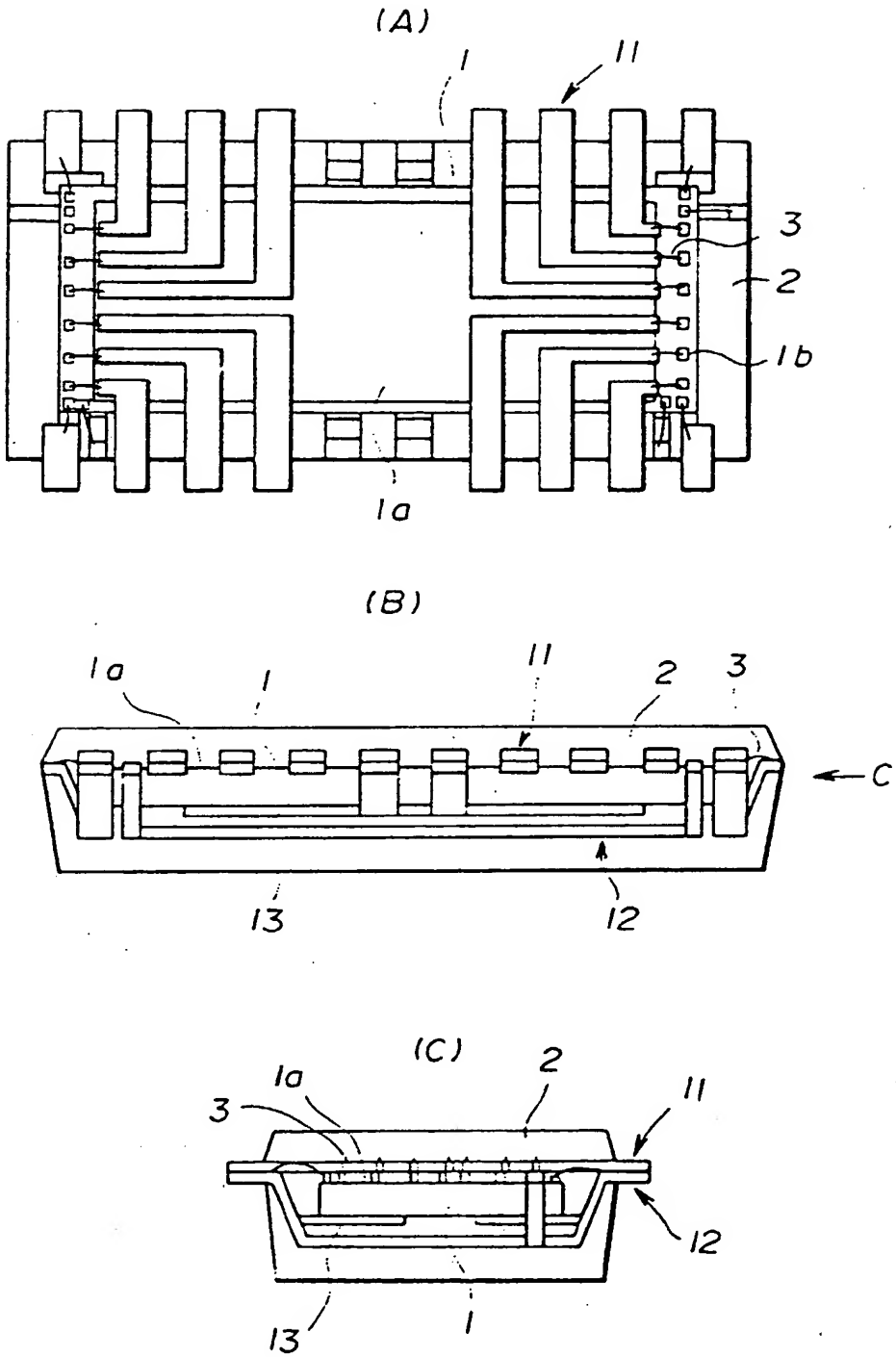
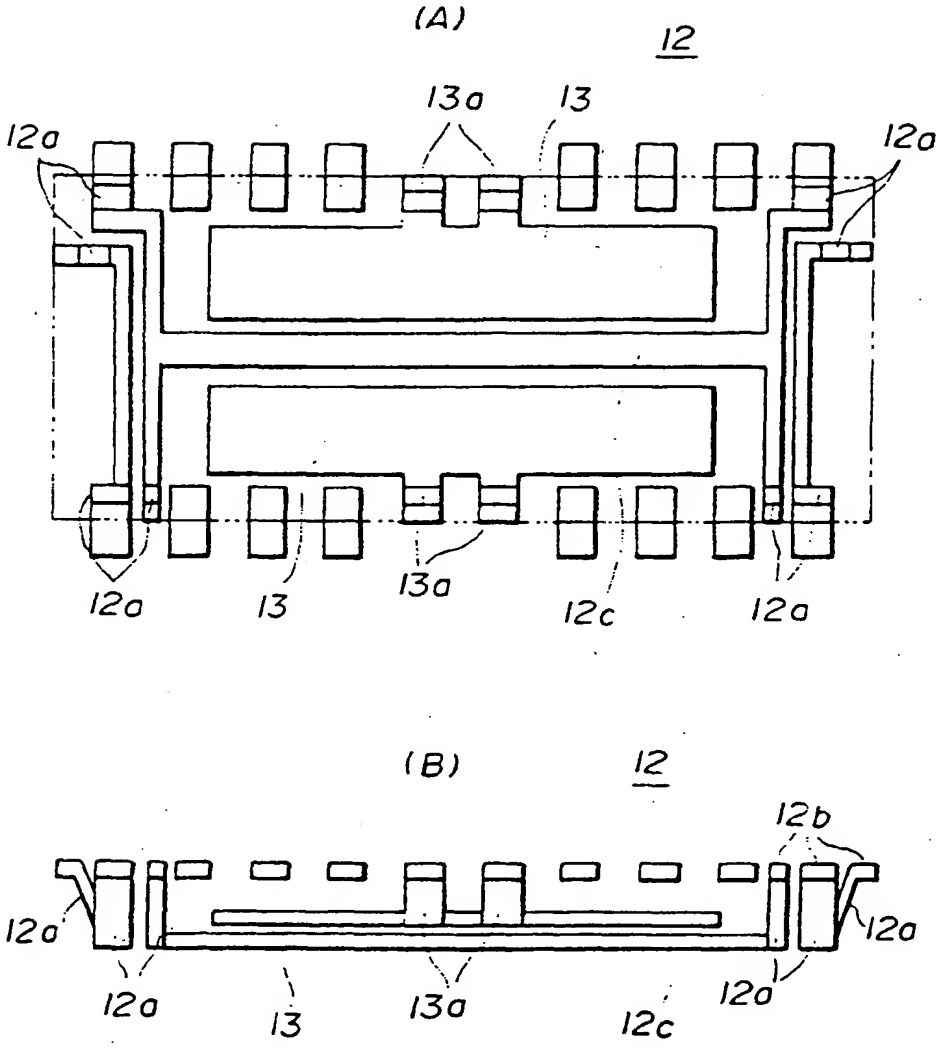


FIG.5


(A)
12
13a
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12a
12a
12a
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13a
12c
12a
(B)
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12a
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12c
12a

FIG.6

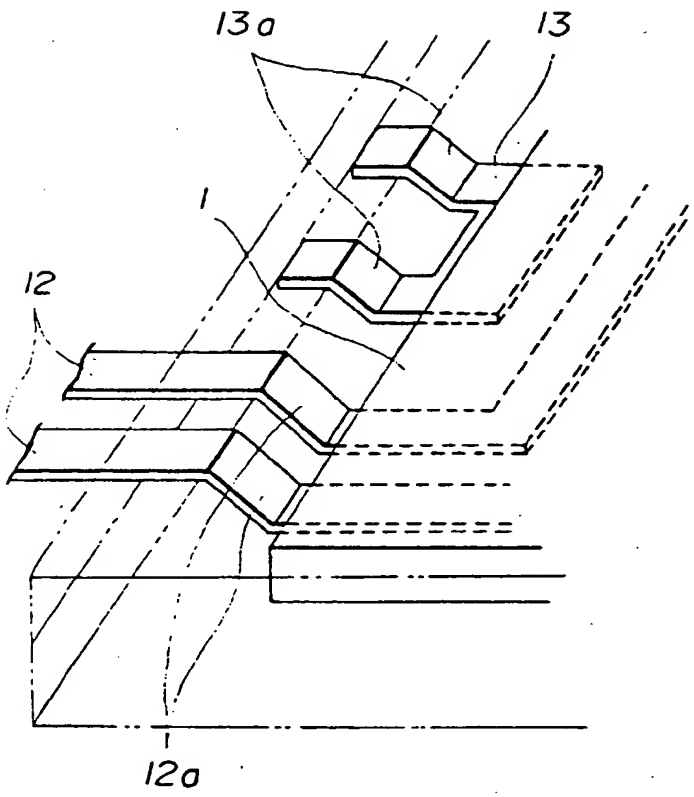


FIG.7

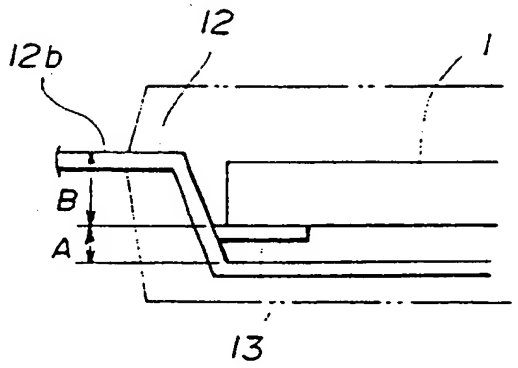


FIG.8

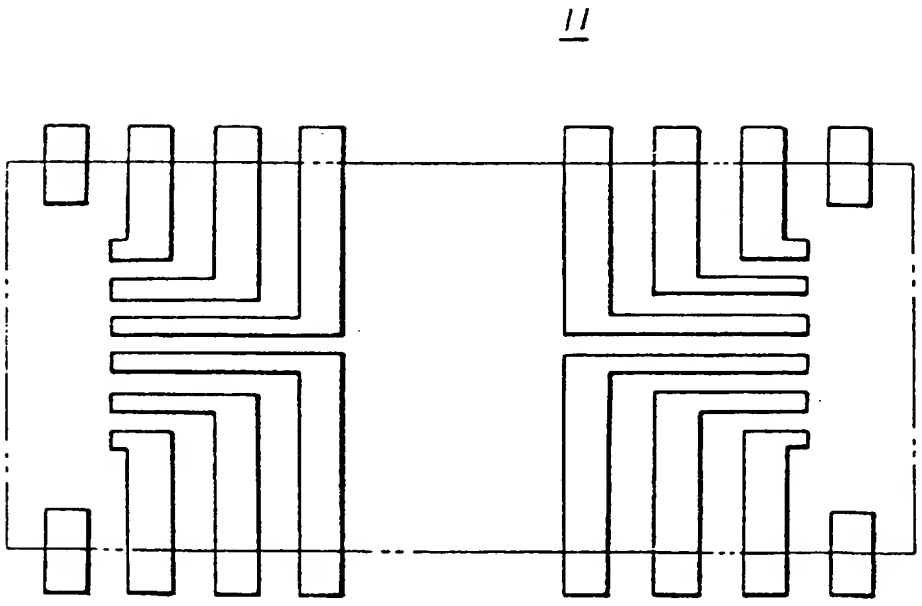


FIG. 9

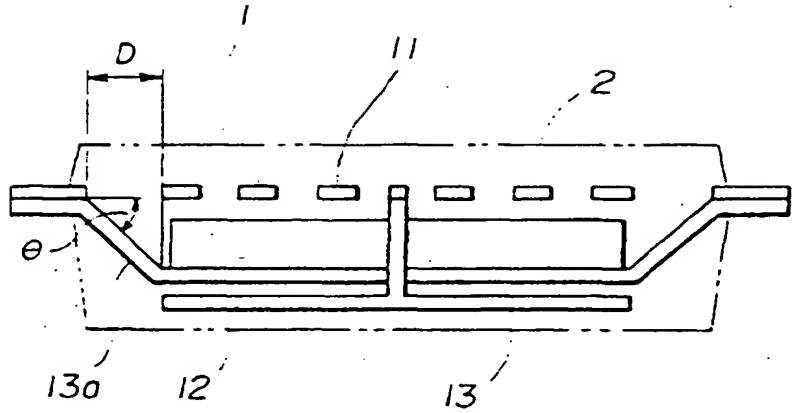


FIG. 10

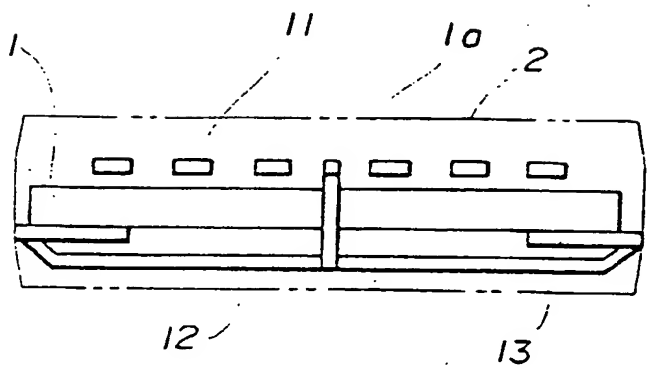


FIG. 11

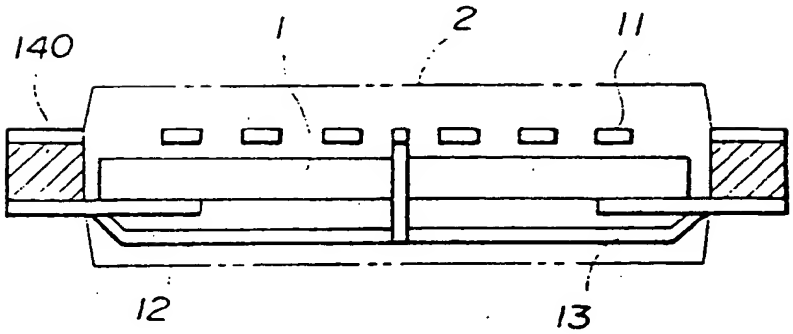


FIG.12

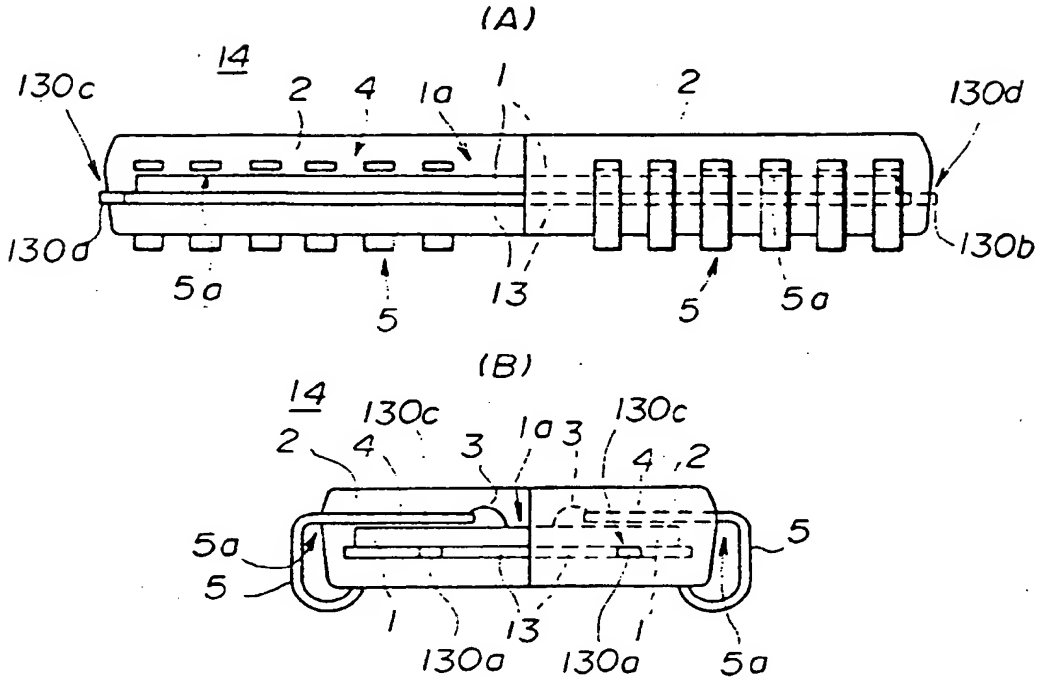


FIG.13

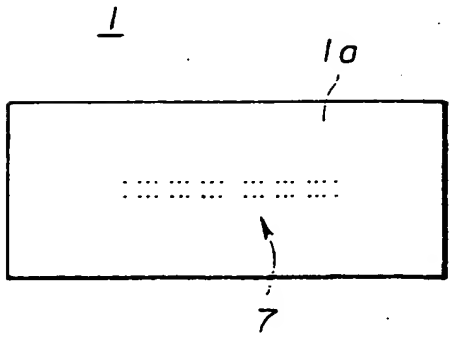
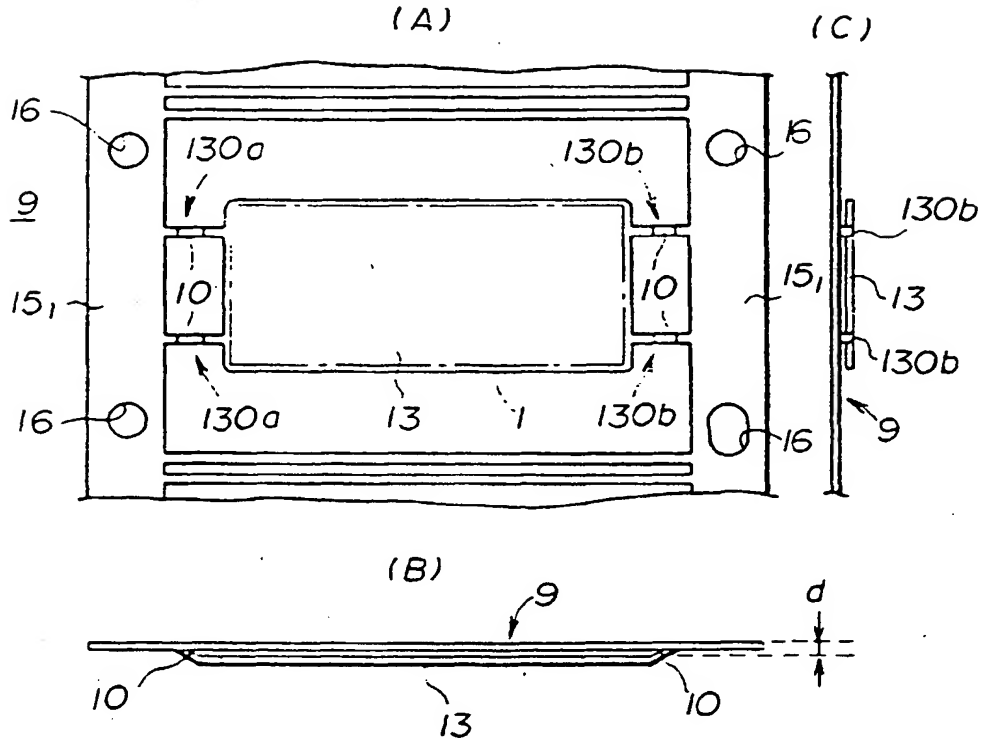


FIG. 14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(C)
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(B)
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10

FIG. 15

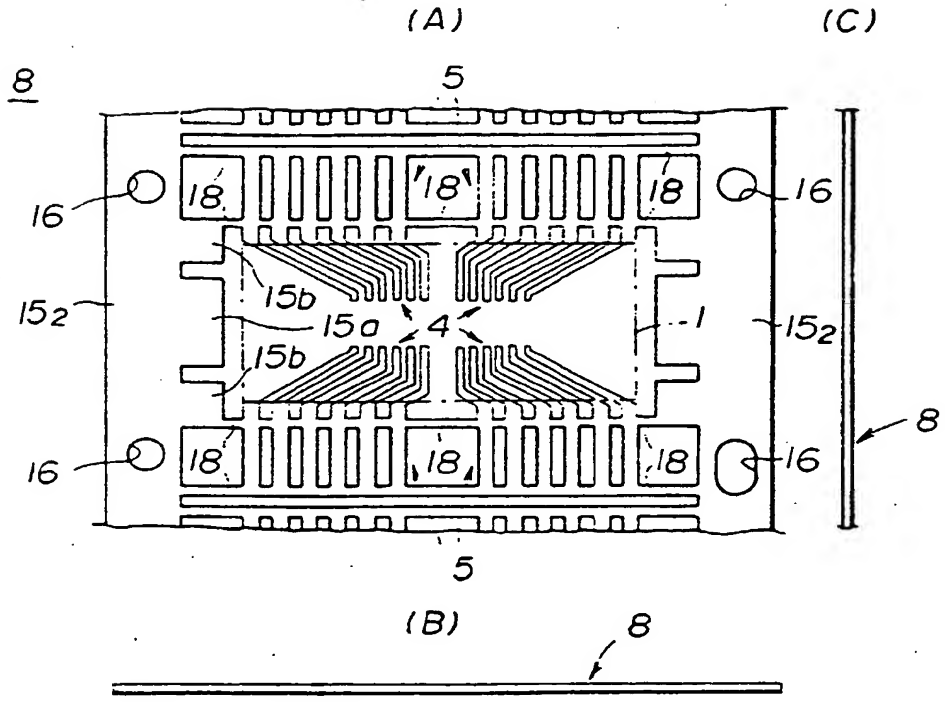


FIG.16

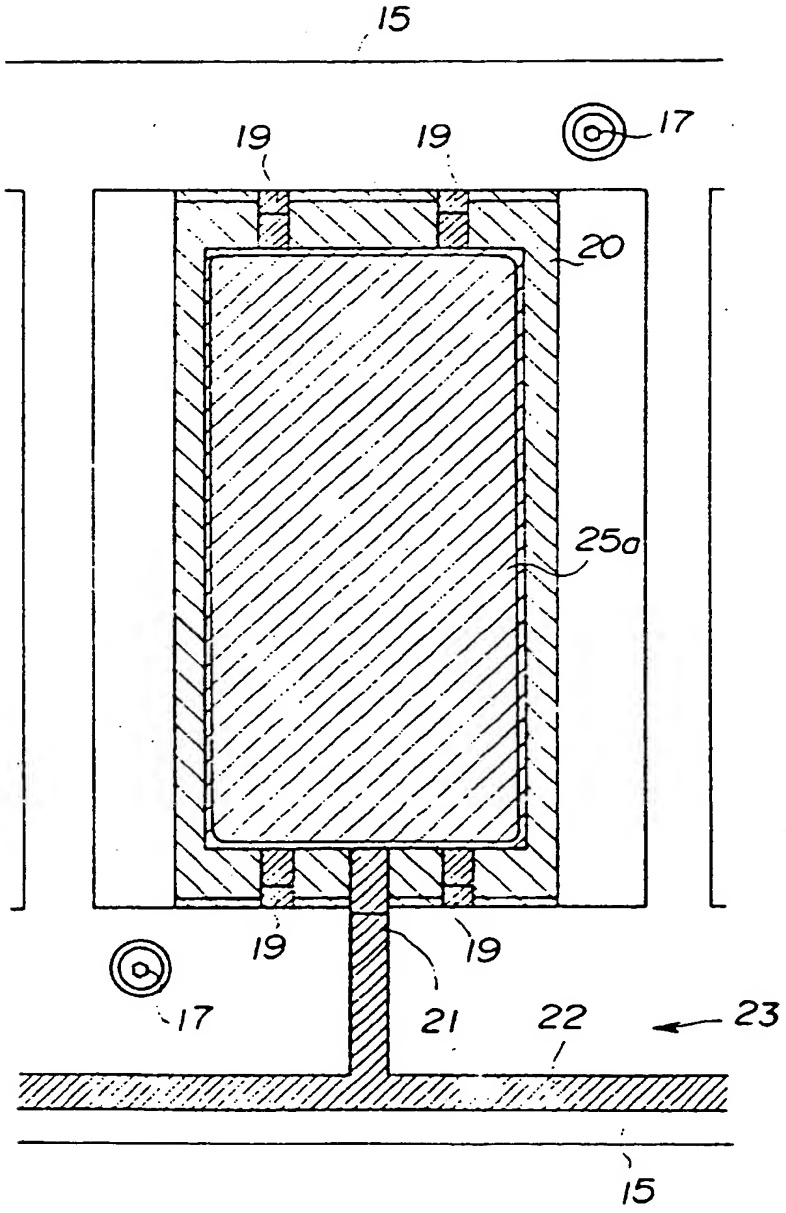


FIG.17

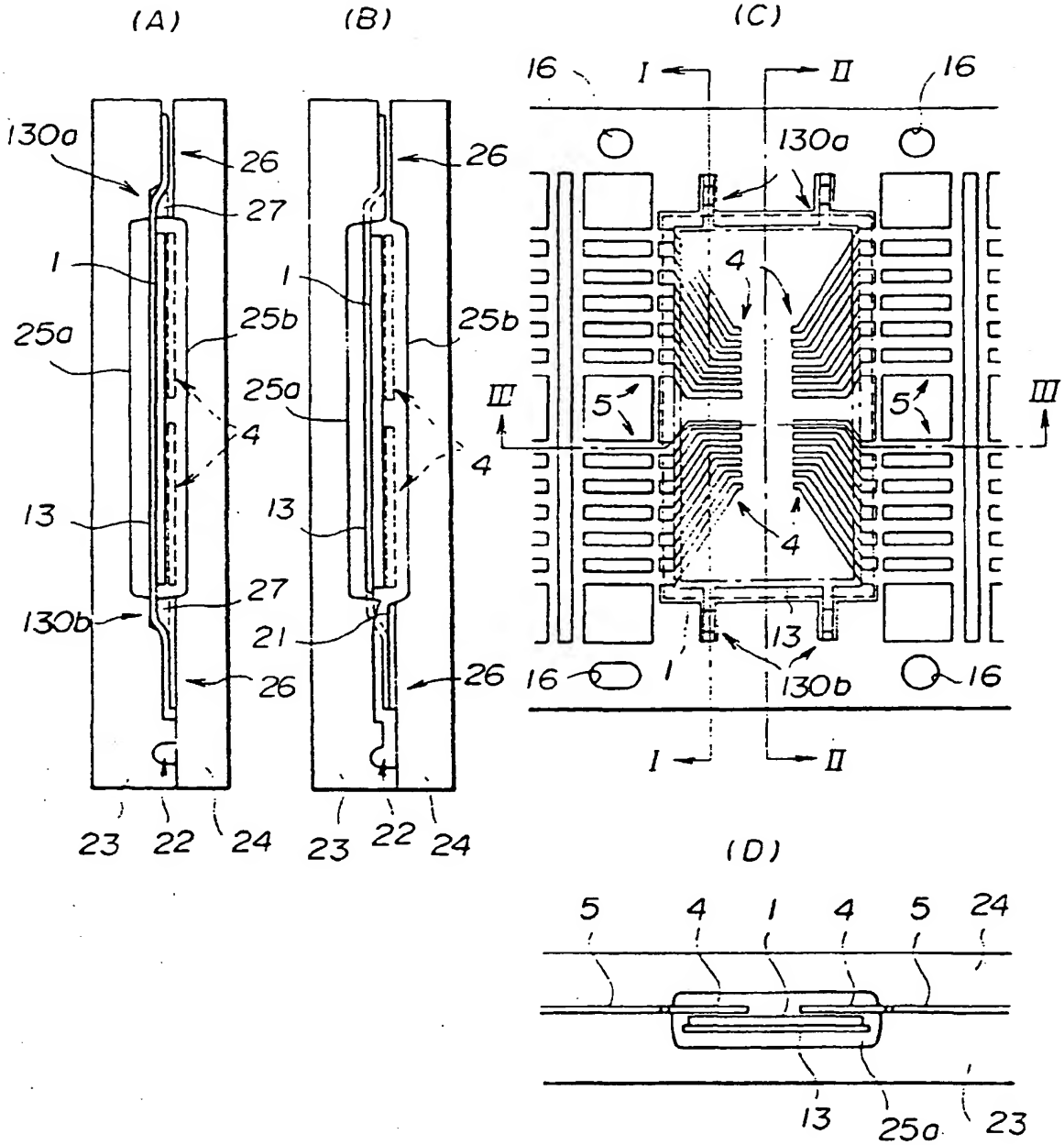


FIG. 18

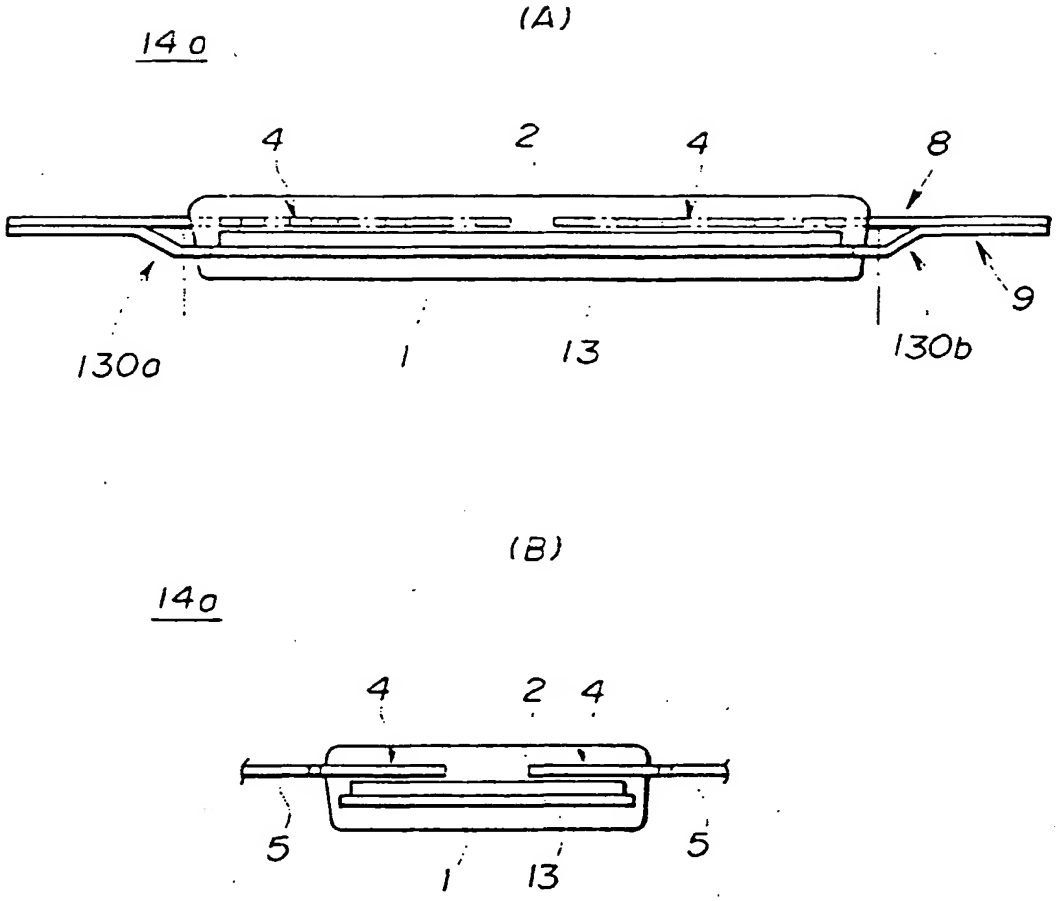


FIG.19

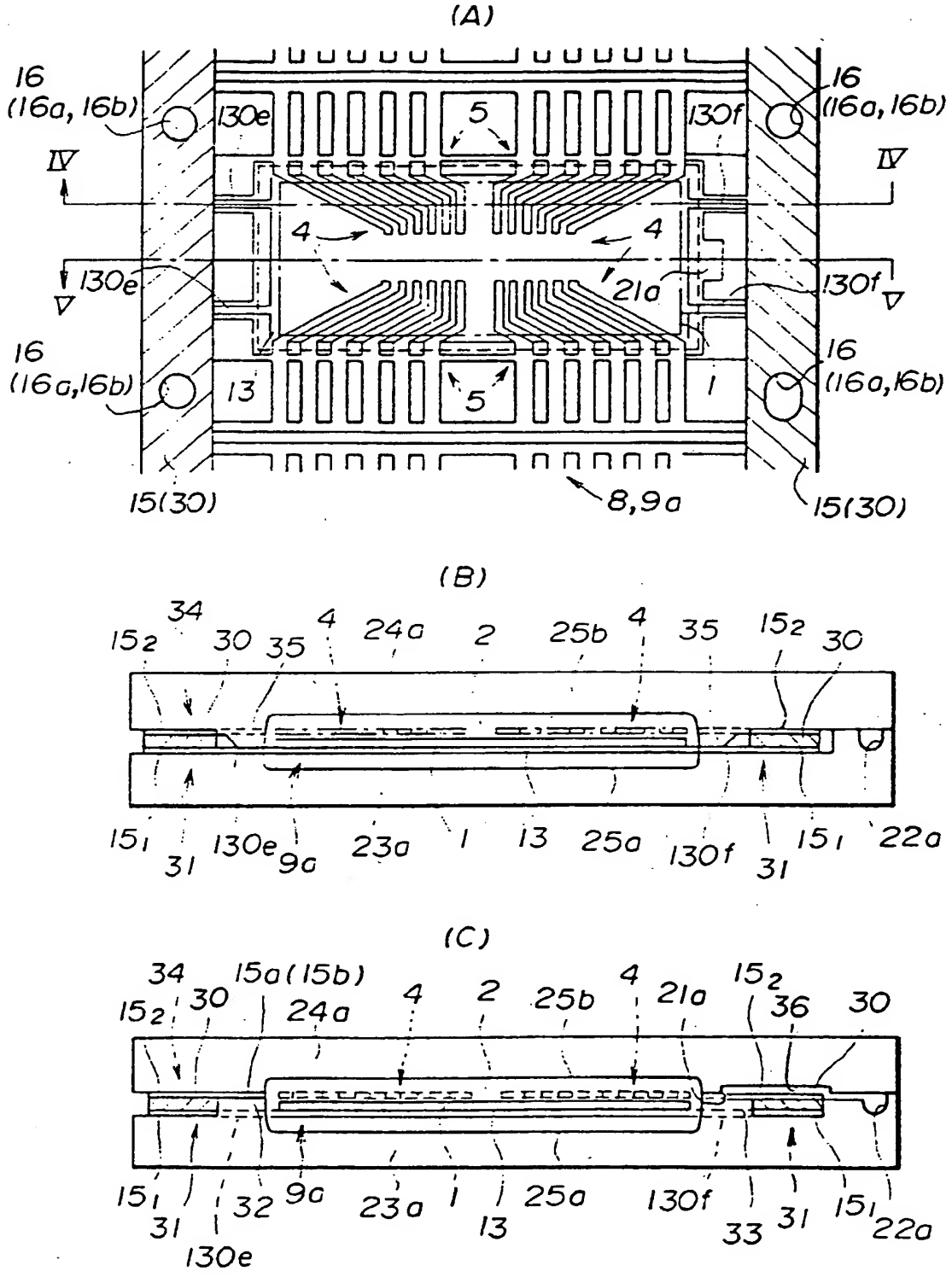
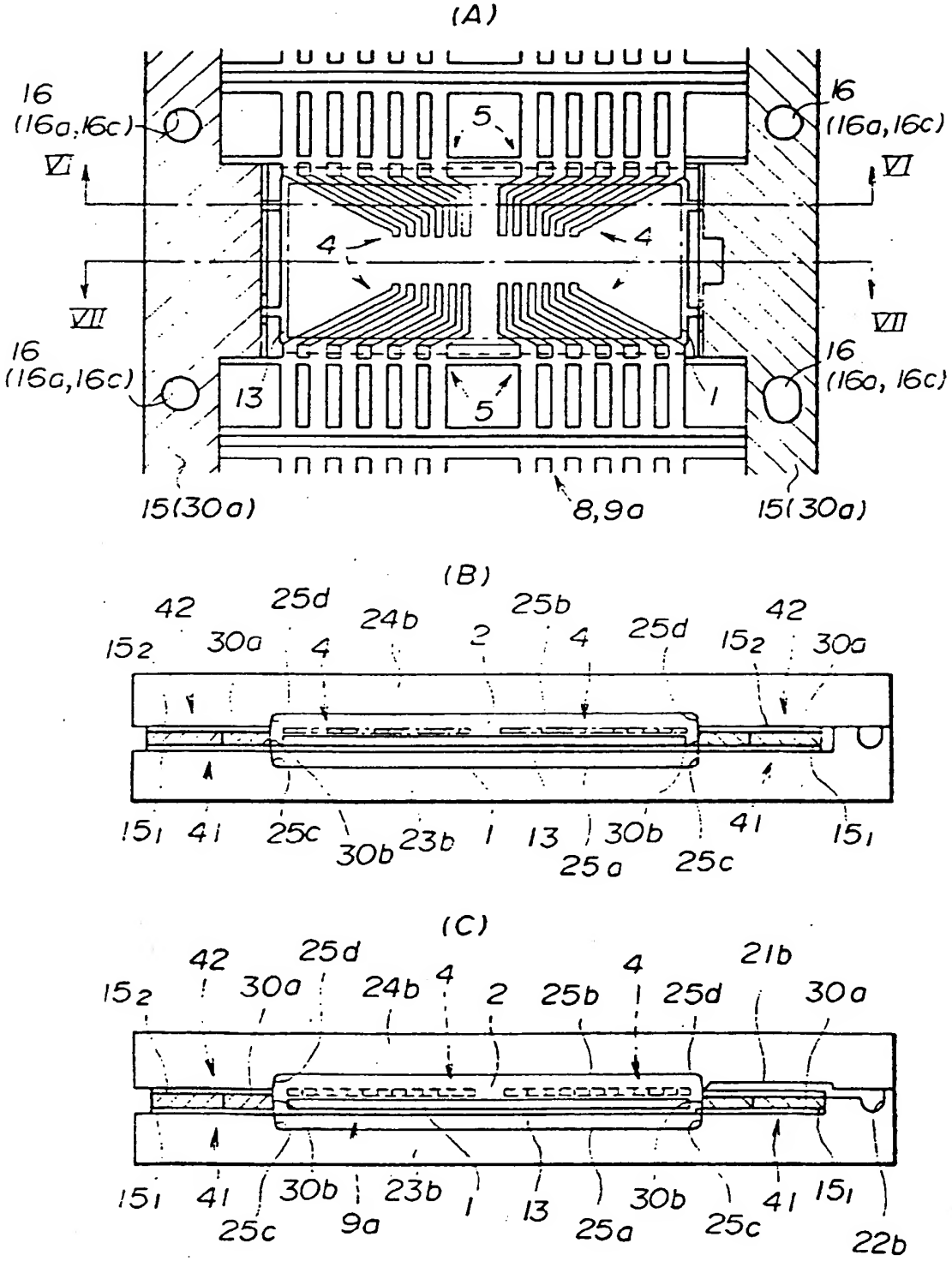


FIG.20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VI
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25a
(C)
21b
9a
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FIG. 21

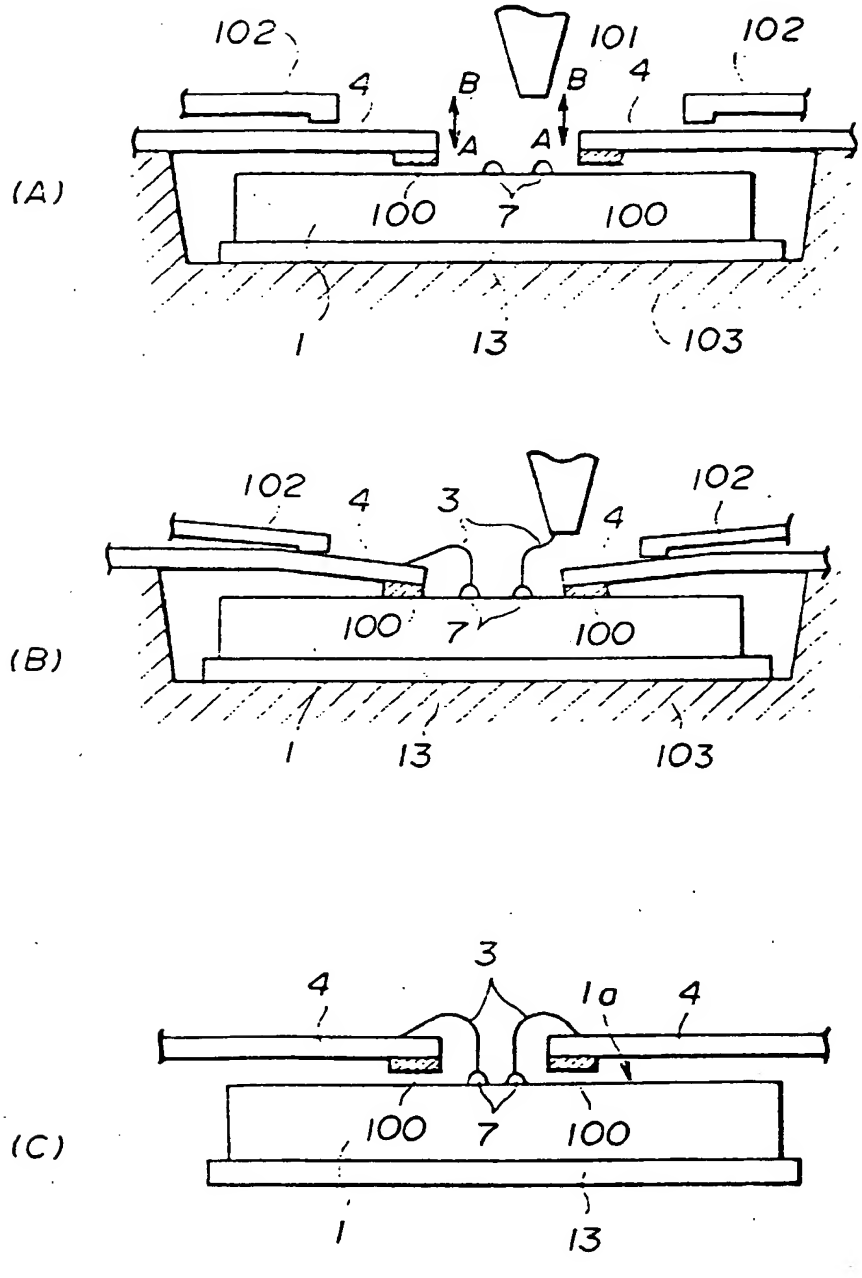
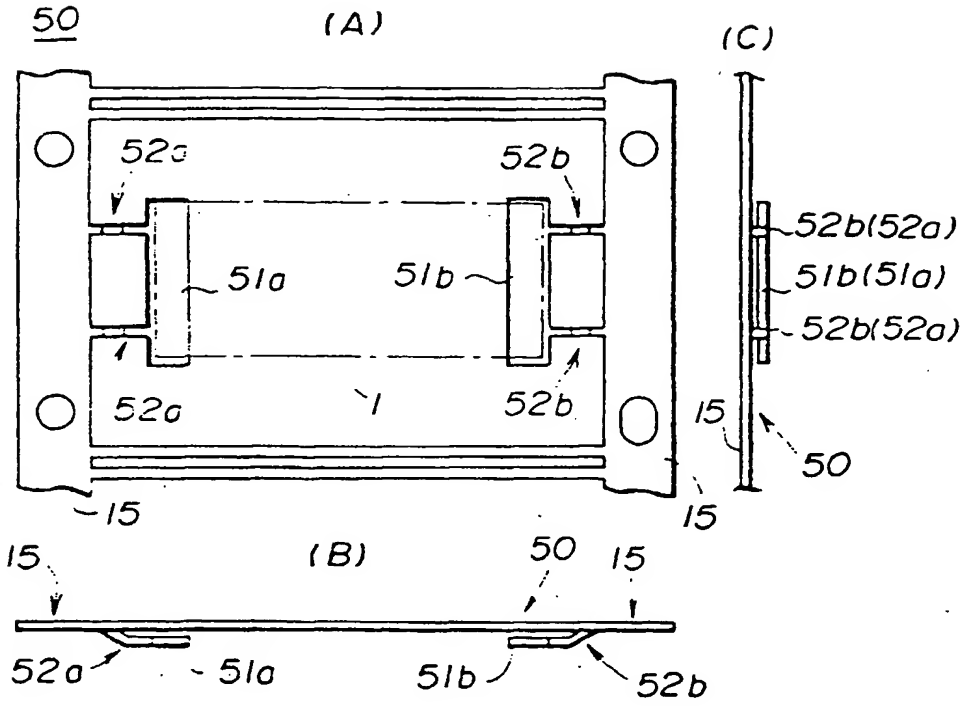


FIG.22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(C)
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51b(51a)
52b(52a)
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50
15
15
(B)
50
15
52a
51a
51b
52b

FIG.23

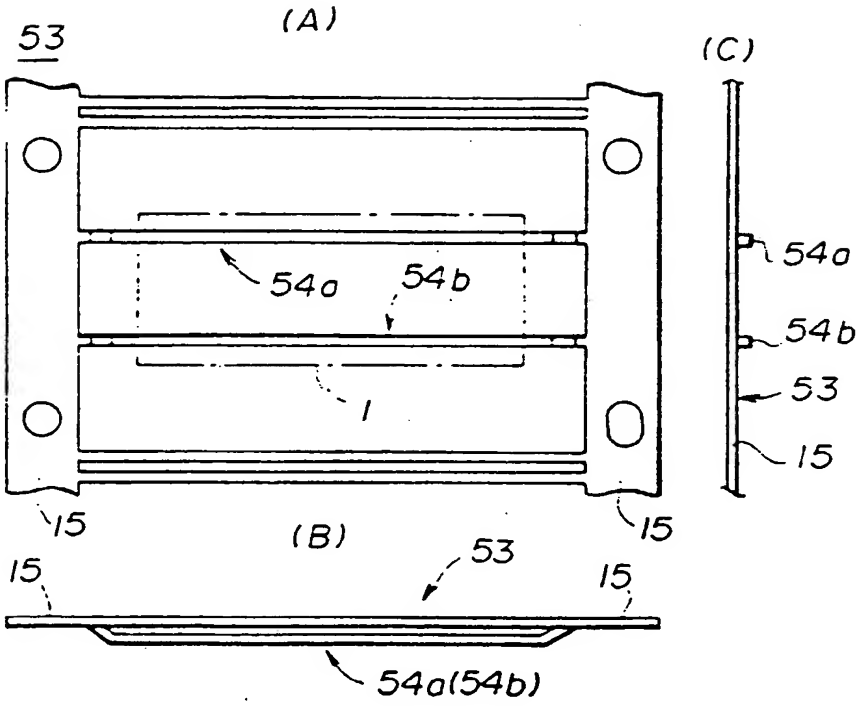
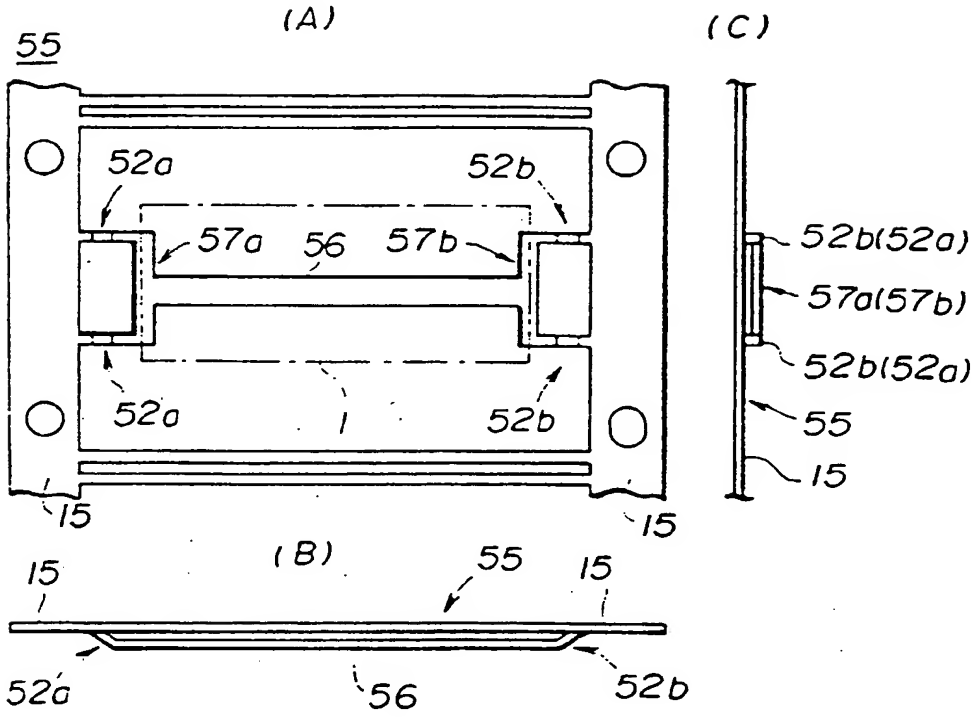


FIG. 24


(A)
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(C)
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(B)
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52a
56
52b

FIG. 25

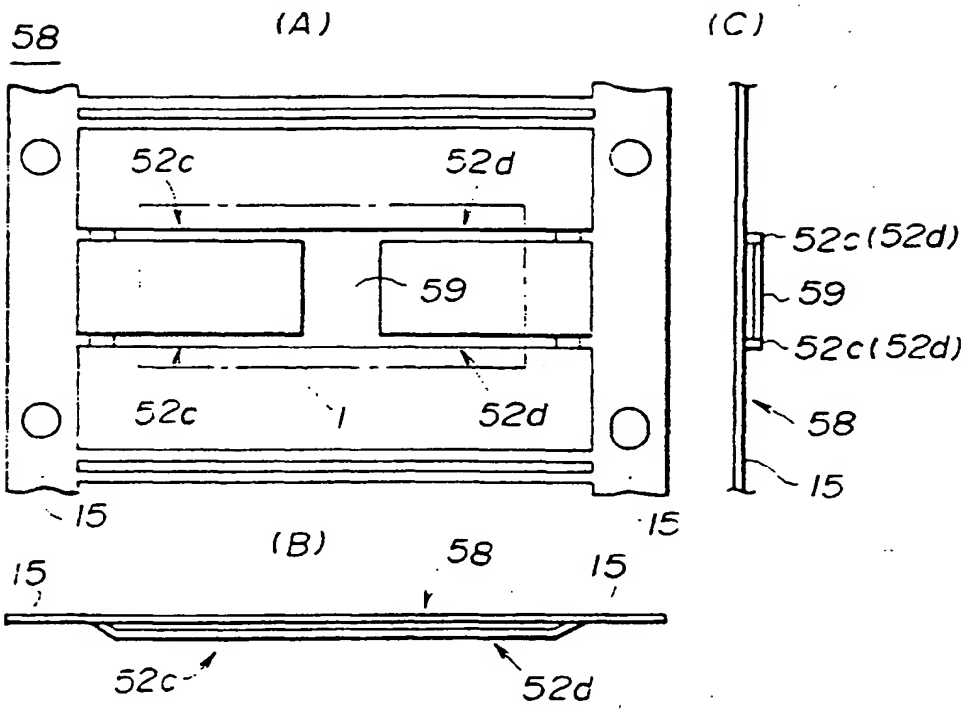


FIG.26

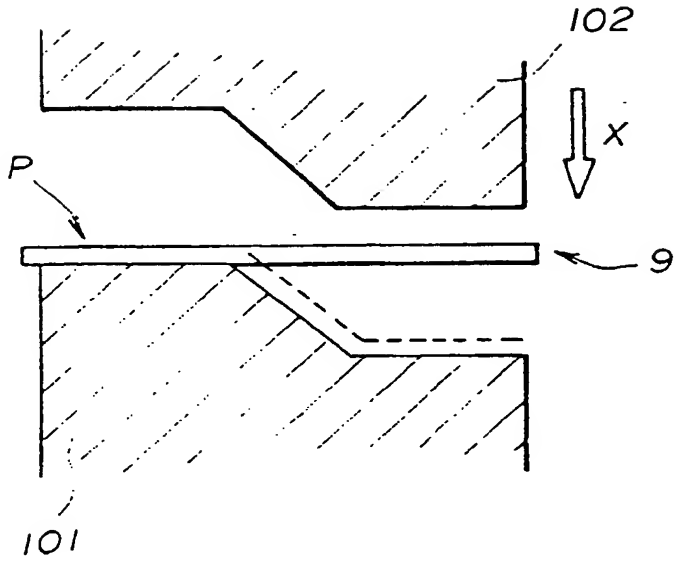


FIG.27

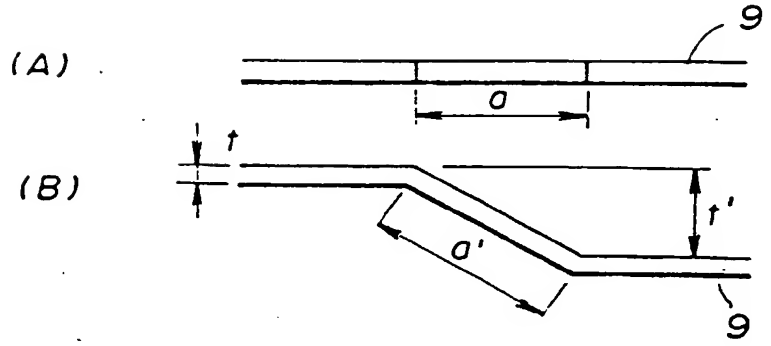


FIG. 28

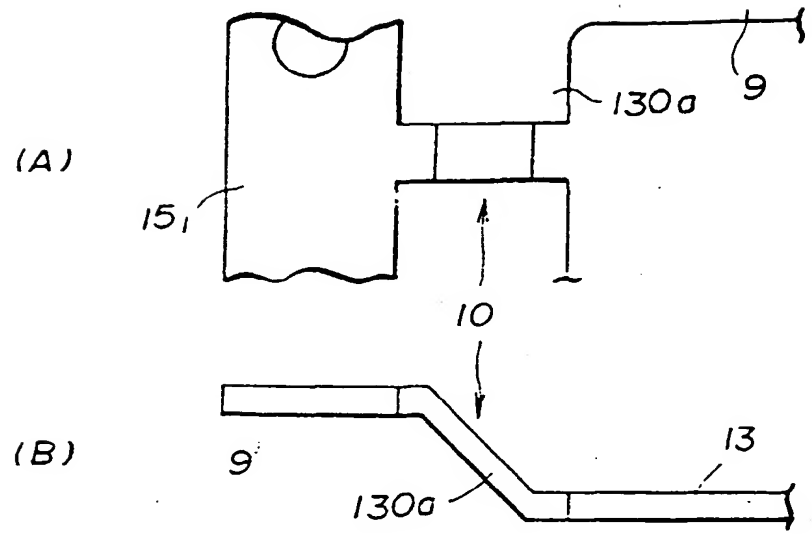


FIG. 29

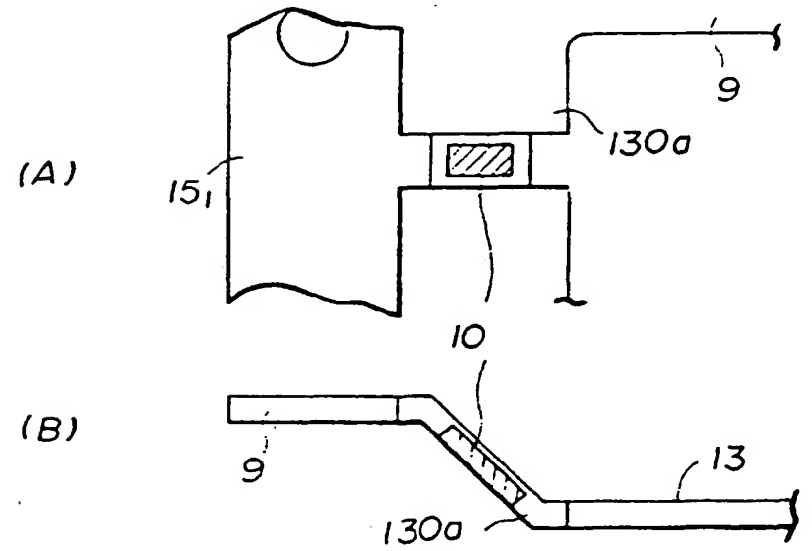


FIG.30

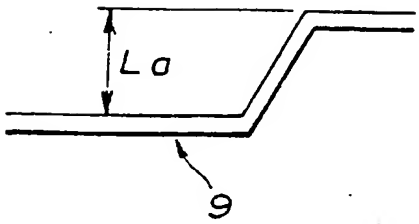


FIG.31

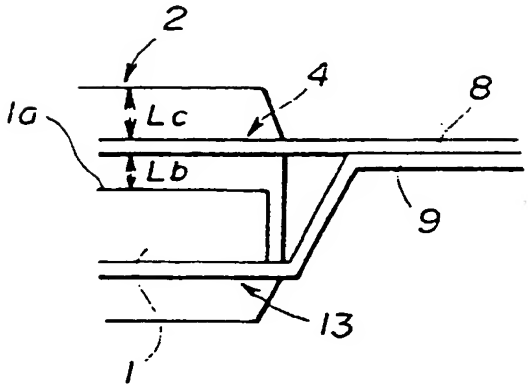


FIG.32

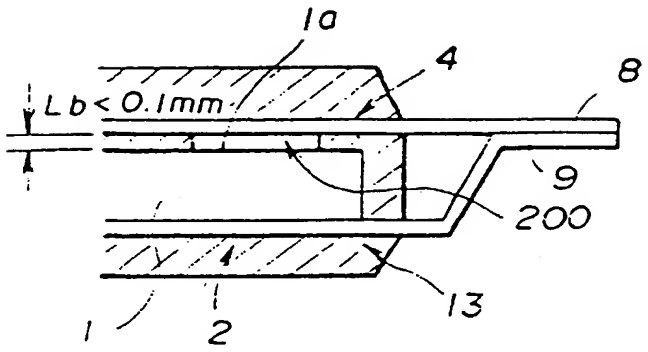


FIG.33

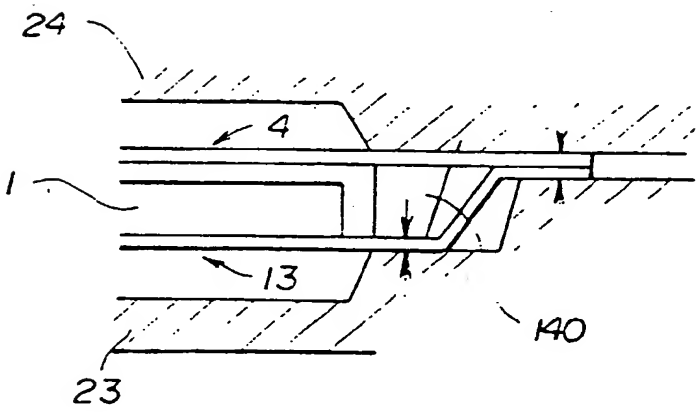


FIG.34

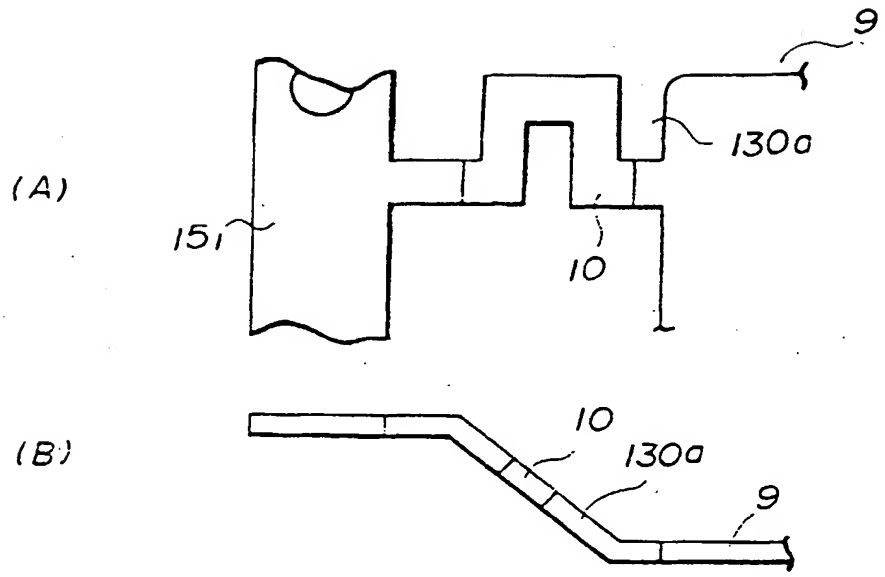


FIG.35

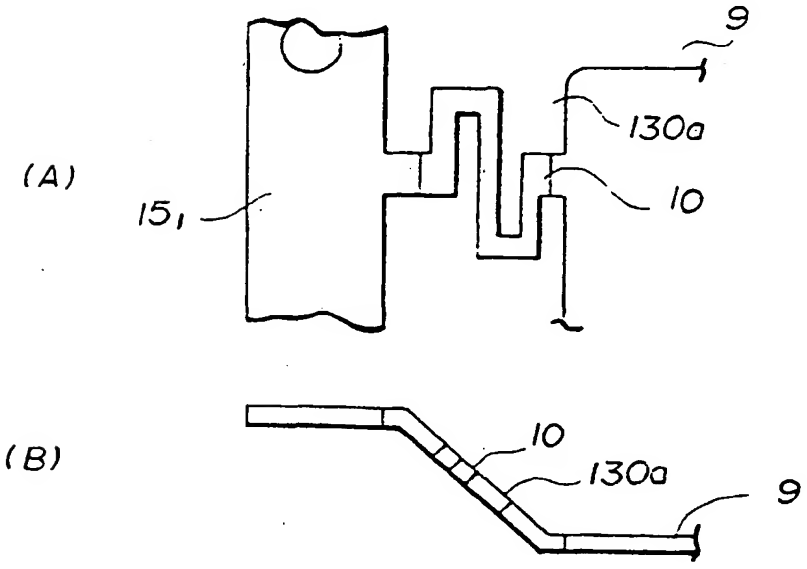


FIG. 36

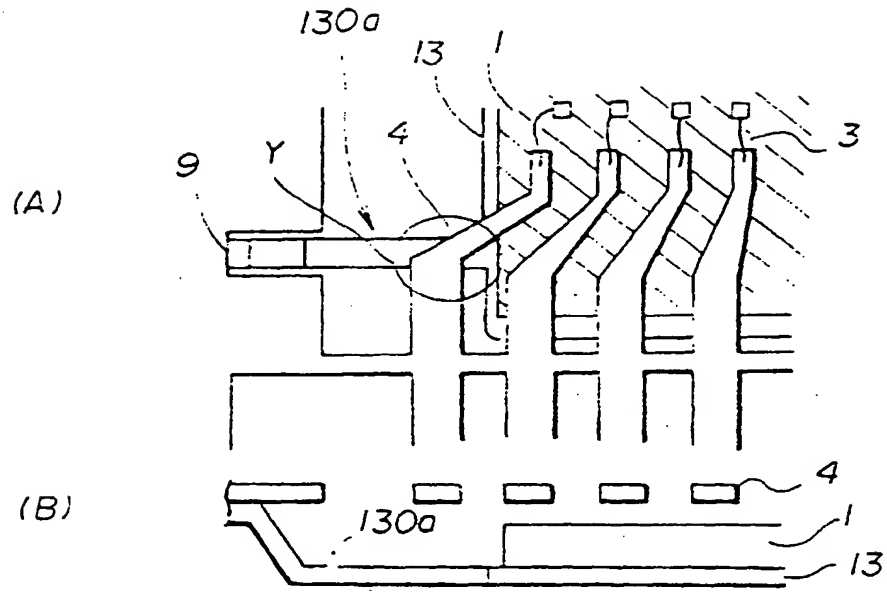
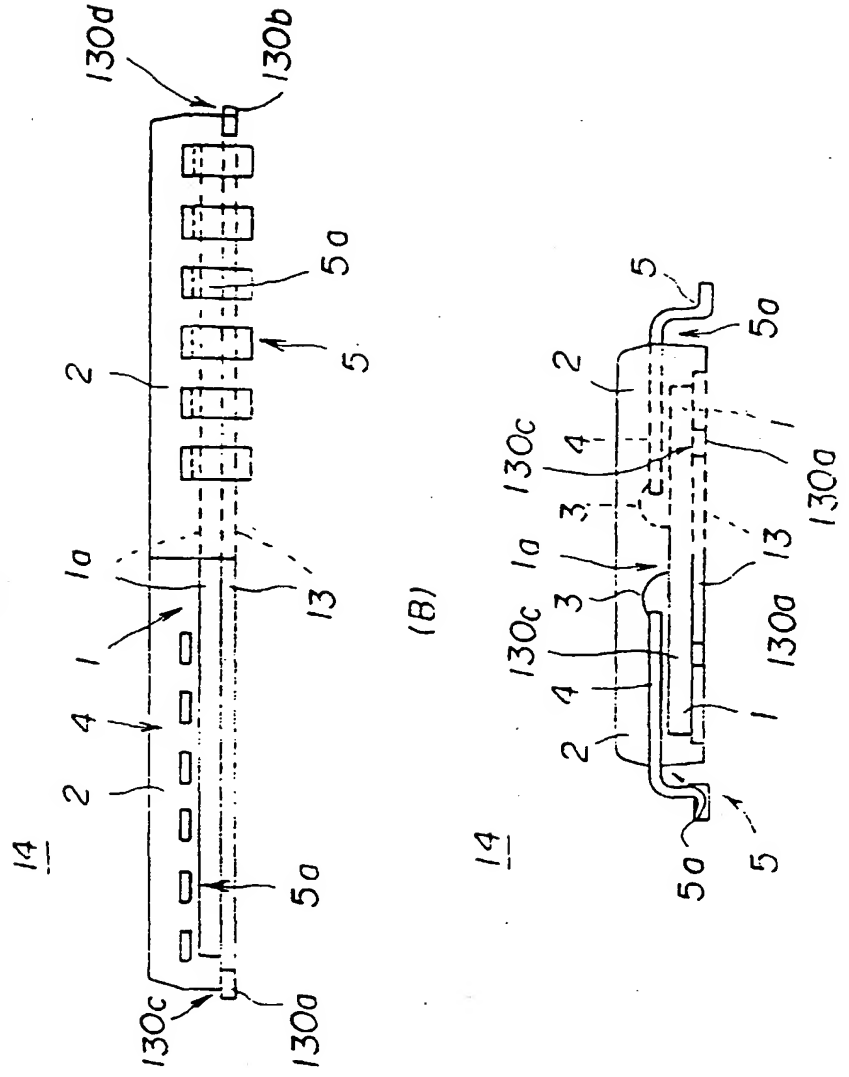


FIG. 37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130a
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5a
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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 987 758 A3

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(43) Date of publication A2:
22.03.2000 Bulletin 2000/12

(21) Application number: **99123357.8**

(22) Date of filing: **23.12.1992**

(51) Int. Cl.[7]: **H01L 23/495**, H01L 21/56

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **27.12.1991 JP 34728391**
14.04.1992 JP 9452492

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
92121907.7 / 0 550 013

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  Kagoshima, 895-14 (JP)

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  c/o Fujitsu Limited
  Kawasaki-shi, Kanagawa 211-8588 (JP)
- **Yoshimoto, Masanori,**
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  Kawasaki-shi, Kanagawa 211-8588 (JP)
- **Takeshita, Kouichi,**
  c/o Kyushu Fujitsu Elect. Ltd.
  Satsuma-gun, Kagoshima 895-14 (JP)

(74) Representative:
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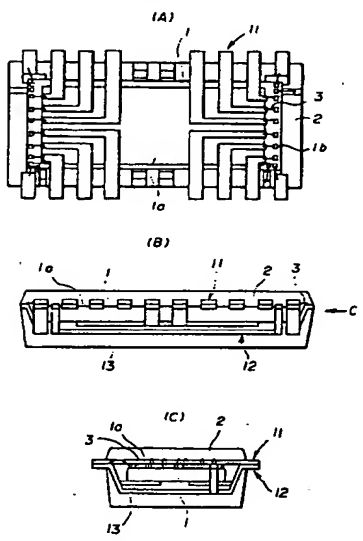
Mitscherlich & Partner,
Patent- und Rechtsanwälte,
Sonnenstrasse 33
80331 München (DE)

(54) Semiconducter device and method of producing the same

(57) A semiconductor device includes a semiconductor chip (1) having top and bottom surfaces, upper leads (11) electrically coupled to the semiconductor chip, where a first gap is formed between the upper leads and the top surface (1a) of the semiconductor chip, lower leads (12) electrically coupled to the semiconductor chip, where a second gap is formed between the lower leads and the bottom surface of the semiconductor chip, and an encapsulating resin (2) which encapsulates the semiconductor chip so as to maintain the first and second gaps.

FIG.4



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EUROPEAN SEARCH REPORT

Application Number
EP 99 12 3357

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 March 2000	Zeisler, P

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L : document cited for other reasons

& : member of the same patent family, corresponding document

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EUROPEAN SEARCH REPORT

Application Number
EP 99 12 3357

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 March 2000	Zeisler, P

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& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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